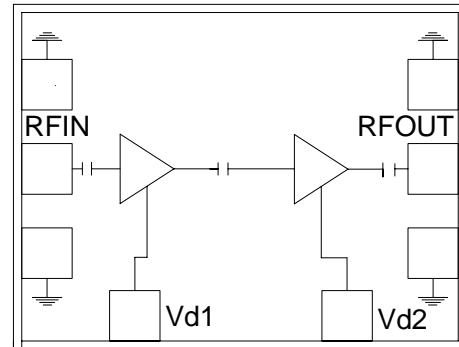


2.7 - 3.7 GHz Low Noise Amplifier

Features

- ◆ Frequency Range : 2.7 – 3.7GHz
- ◆ Low Noise Figure < 1.4 dB
- ◆ 26 dB High gain
- ◆ 18 dBm Medium Power output
- ◆ High IP3
- ◆ Input Return Loss > 5 dB
- ◆ Output Return Loss > 15 dB
- ◆ Single supply operation
- ◆ No external matching required
- ◆ DC decoupled input and output
- ◆ 0.15 μm InGaAs pHEMT Technology
- ◆ Chip dimension: 2.7 x 2.1 x 0.1 mm

Functional Diagram



Typical Applications

- ◆ RADAR
- ◆ Military & space
- ◆ VSAT

Description

The AMT2122051 is S-band Low noise amplifier with a medium power output. The LNA uses 2 stages of amplification and operates in 2.7 – 3.7 GHz frequency range. The LNA features 26 dB of gain with a low noise figure of 1.4 dB and typical input and output return losses of 5 dB and 15 dB respectively. The LNA is unique in delivering a medium power output of 18 dBm. This feature enables it to be used in high gain applications with enhanced linearity requirements. The chip operates from a single positive supply voltage. The die is fabricated using a reliable 0.15 μm InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings⁽¹⁾

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+6	volts
RF input power (RFin at Vd=4V)	18	dBm
Operating temperature	-50 to +85	°C
Storage Temperature	-65 to +150	°C

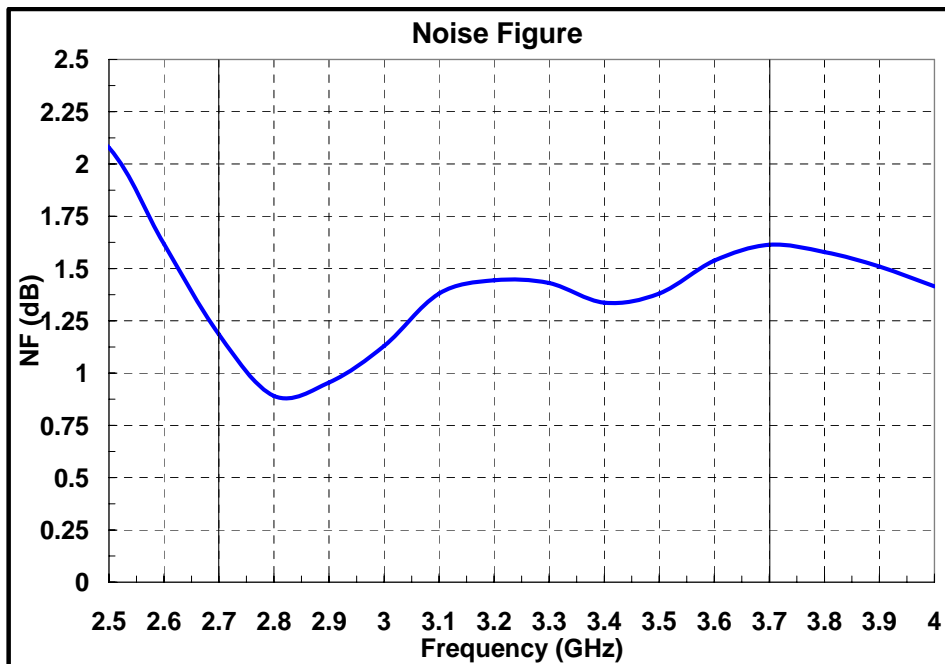
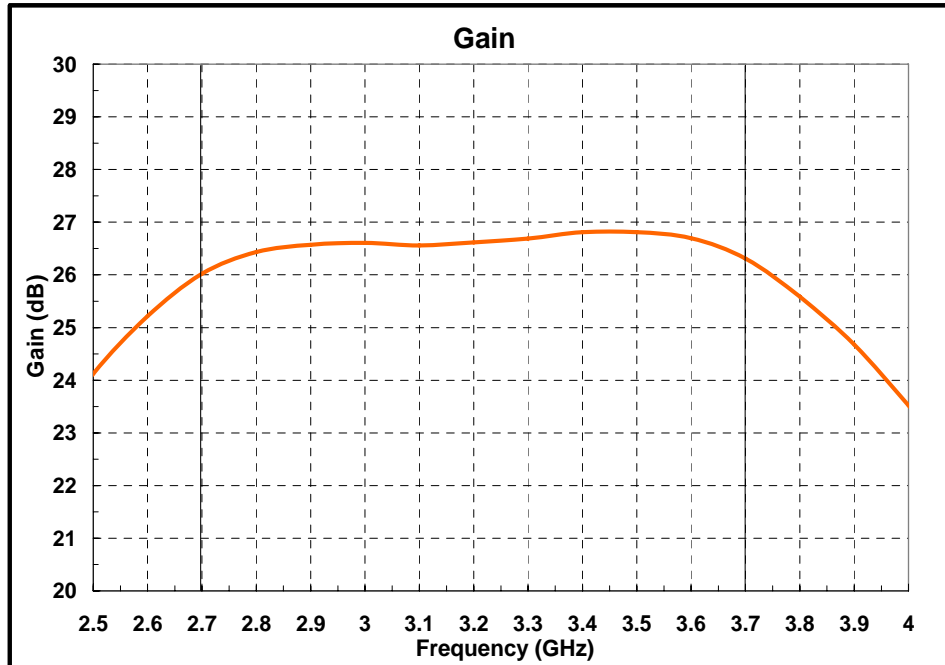
1. Operation beyond these limits may cause permanent damage to the component

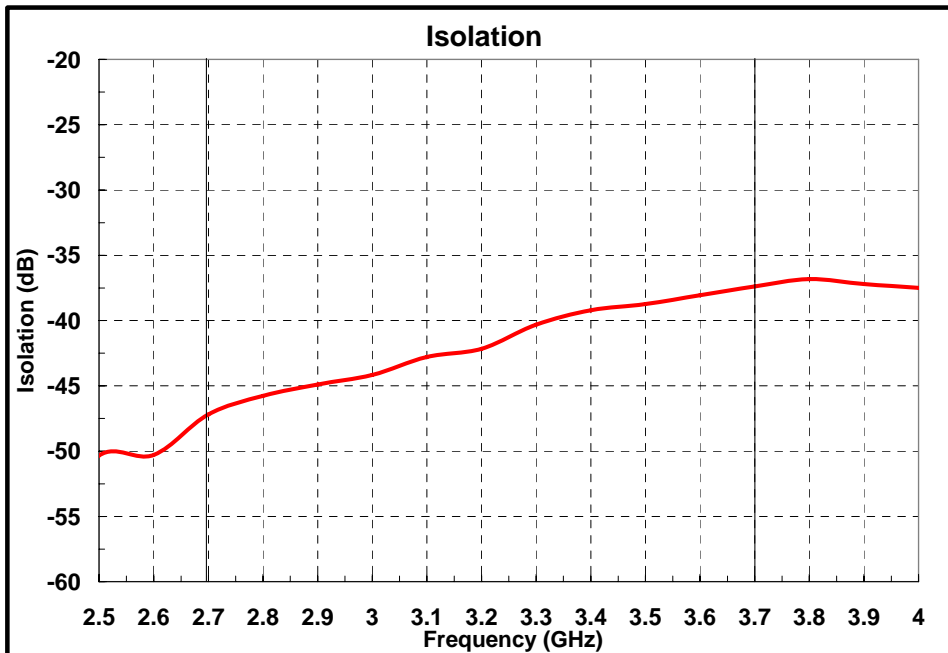
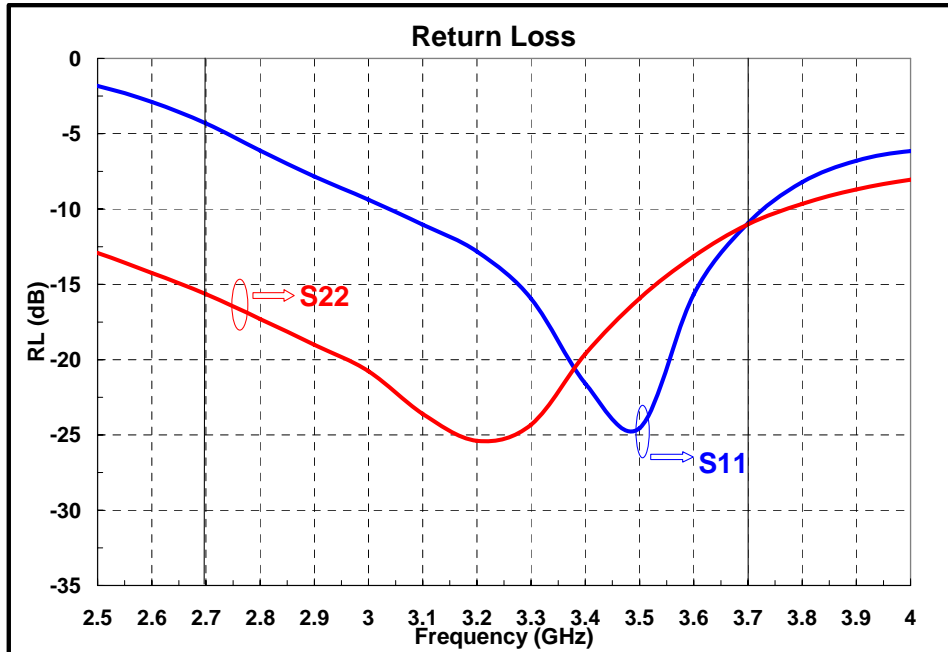
Electrical Specifications⁽¹⁾ @ T_A = 25 °C, V_{d1} = V_{d2} = 4V Z_o = 50 Ω

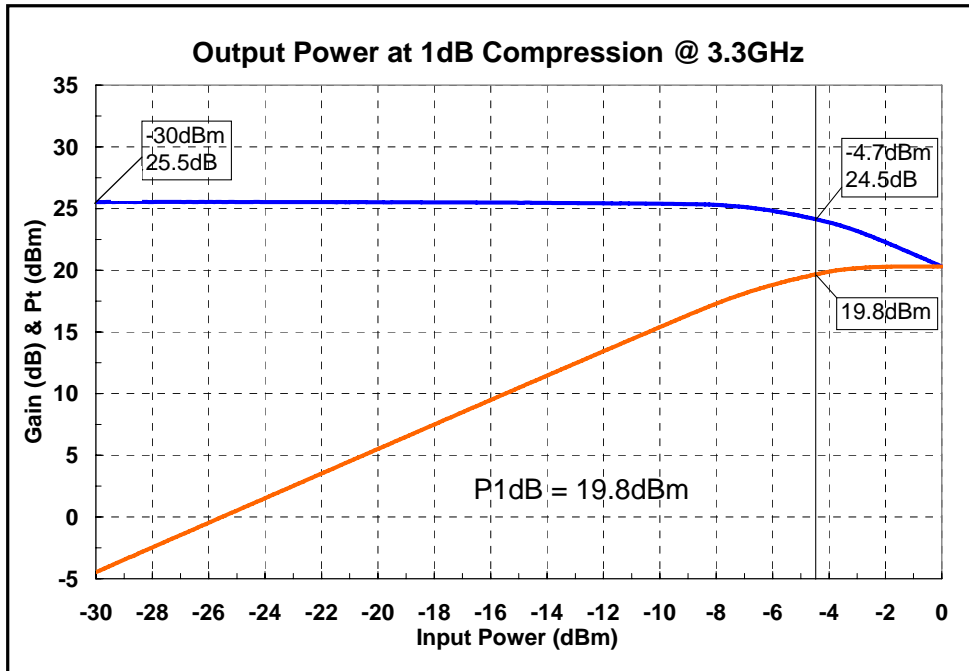
Parameter	Typ.			Units
Frequency Range	2.7 – 3.1	3.1 – 3.5	2.7 - 3.7	GHz
Gain	26	26.5	26.5	dB
Gain Flatness	+0.5	± 0.2	± 0.5	dB
Noise Figure	1.4	1.4	1.6	dB
Input Return Loss	5	11	5	dB
Output Return Loss	15	15	12	dB
Output Power (P1 dB)	18	19	18	dBm
Saturated output power (Psat)	-	21	-	dBm
Output Third Order Intercept (IP3)	-	30	-	dBm
Supply Current	-	110	-	mA

Note:

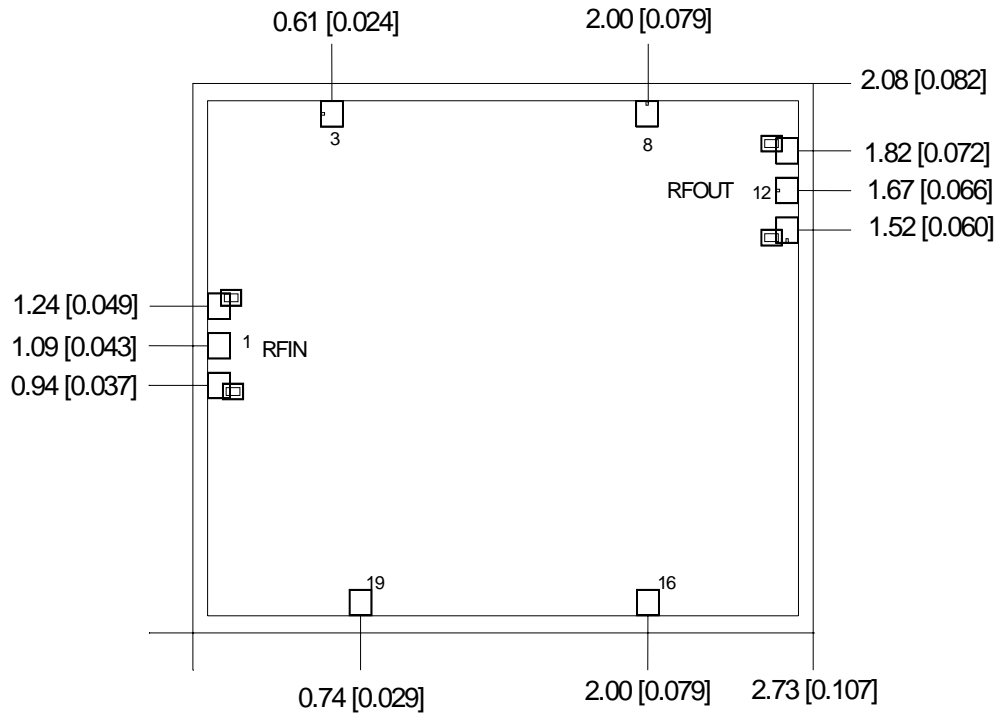
1. Electrical specifications are measured in a test fixture.

Test fixture data $V_{d1}=V_{d2} = 4V$, Total Current =110ma, $T_A = 25^\circ C$ 

Test fixture data
 $V_{d1}=V_{d2} = 4V$, Total Current =110ma, $T_A = 25^\circ C$


Test fixture data
 $V_{d1}=V_{d2} = 4V$, Total Current = 110ma, $T_A = 25^\circ C$


Mechanical Characteristics



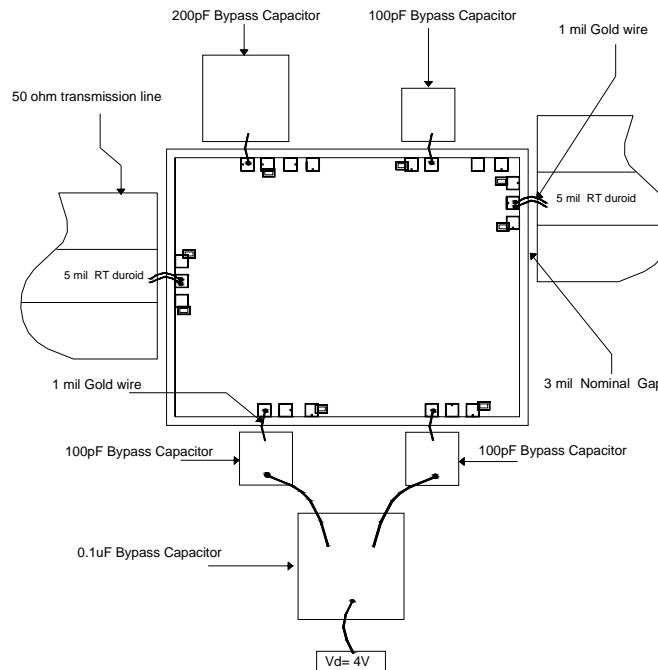
Units: Millimeters [Inches]

All RF and DC bond pads are 100 μ m x 100 μ m

Note:

1. Pad no. 19: Vd1
2. Pad no. 16: Vd2
3. Pad no. 3 : 1st stage source bypass
4. Pad no. 8 : 2nd stage source bypass
5. Pad no. 1 : RF Input
6. Pad no. 12 : RF Output

Recommended Assembly Diagram



Note:

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF capacitor.
3. Input and output 50 ohm lines are on 5 mil substrate.
4. 0.1 μ F capacitors may be additionally used as a second level of bypass for reliable operation.

Die attach: For Epoxy attachment, use of a two-component conductive epoxy is recommended. An epoxy fillet should be visible around the total die periphery. If Eutectic attachment is preferred, use of fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200 μ m length of wedge bonds is advised. Single Ball bonds of 250-300 μ m though acceptable, may cause a deviation in RF performance.



GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice