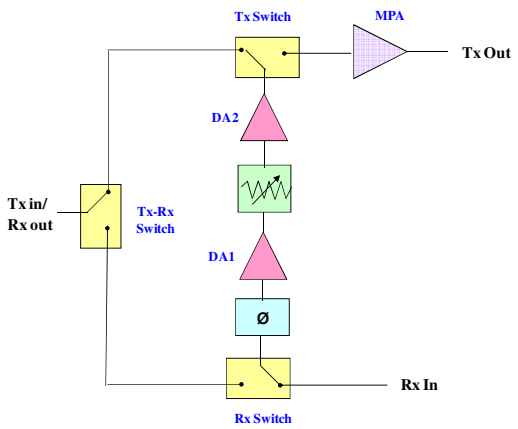
9 - 10 GHz GaAs MMIC Core Chip

Features

- **Frequency Range: 9GHz – 10GHz**
- **Tx Small Signal Gain: 28dB**
- **Rx Small Signal Gain: 4dB**
- **Tx Output P_{1dB} : 22dBm**
- **Tx Output P_{sat} : 23dBm**
- **Input Return Loss < 12 dB**
- **Output Return Loss < 12 dB**
- **Phase Shifter Range : 6 Bit, 5.625° step**
- **Attenuator Range : 6 Bit, 0.5dB step**
- **0.5 µm InGaAs pHEMT Technology**
- **Chip dimension: 5.3 x 5.3 x 0.1 mm**

Functional Diagram



Typical Applications

- **RADAR**
- **Military & space**
- **VSAT**

Description

The AMT2941031 is a 3 port multi-functional Transmit / Receive core chip. It is designed for applications operating within the 9 GHz to 10 GHz range. This core chip consists of integrated transmit/receive switches, 6-bit phase shifter, 6-bit attenuator, gain blocks and medium power amplifier. The digital control logic allows fast phase shift and attenuation changes. The chip has surface passivation to protect the internal circuit. It also has backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for phased array radar applications.

Absolute Maximum Ratings[1]:

Parameter	Absolute Maximum	Units
Supply Voltage (DA1VD, DA2VD, VDMPA)	6	V
Gate Voltage of MPA (VGMPA)	-0.7 to -2.5	V
Control Logic Supply (5V / 5VOPT1 / 5VOPT2)	0 to 5.5	V
Control Logic Supply & Gate Supply for DA1 and DA2 (-5V / -5VOPT1 / -5VOPT2)	-6 to -4	V
RF input at Tx_{in} Port, Rx_{in} Port	17 @ 85 °C	dBm
Supply current in Tx Mode ($I_{dDA1}+I_{dDA2}+I_{dMPA}$)	400	mA
Supply current in Rx Mode ($I_{dDA1}+I_{dDA2}$)	150	mA
Operating temperature	-40 to +85	°C
Storage Temperature	-65 to +150	°C

1. Operation beyond these limits may cause permanent damage to the component

Test fixture data[2]:

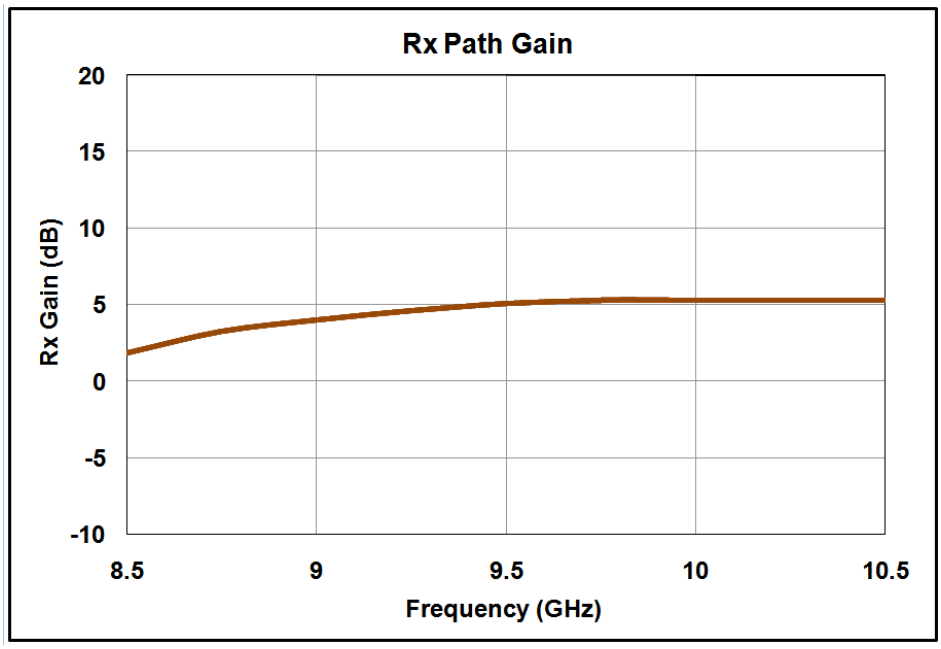
VDDA1 = VDDA2 = VDMPA = 5V; VGMPA=-1V ; T_A = 25 °C

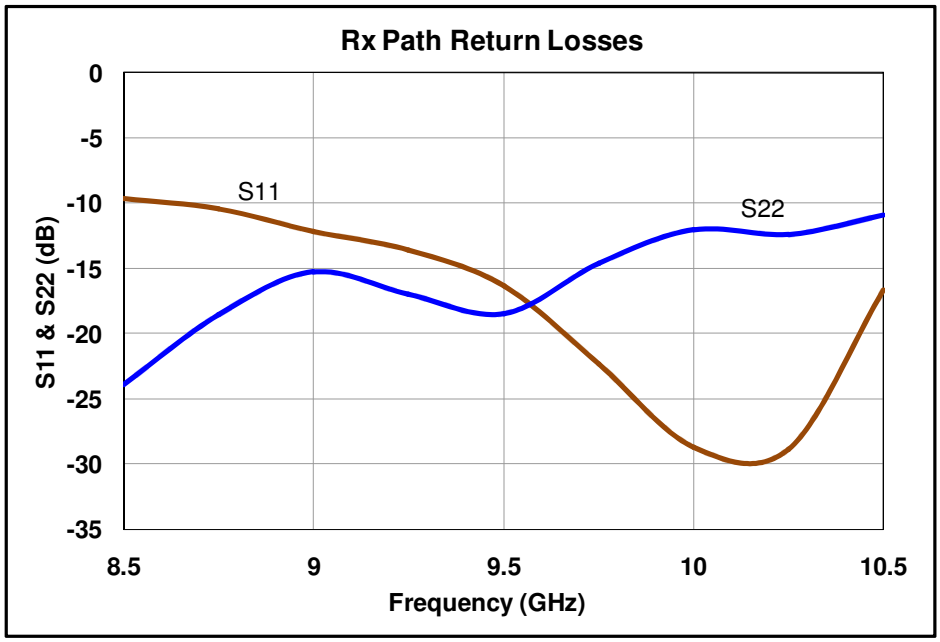
Parameter	Typical Value	Units
Frequency Range	9.0-10.0	GHz
Receive Small Signal Gain	4.0	dB
Transmit Small Signal Gain	28	dB
Transmit Large Signal Gain (@ Pin = 0dBm)	23	dB
Input / Output Return Losses	12	dB
Receive Output Power for 1dB Compression Point	13.5	dBm
Receive Output Third Order Intercept Point	24	dBm
Transmit Output Power for 1dB Compression Point	22	dBm
Transmit Output Saturated Power	23	dBm
Phase Shifter Range (6 Bit, 64 states, 5.625° step)	0 – 355	deg
RMS Phase Error	3	deg
Attenuation Range (6 Bit, 64 states, 0.5dB step)	0 – 31.5	dB
RMS Attenuation Error	0.7	dB
Tx/Rx Switch Isolation	< -57	dB
Supply Voltages	5, -5, -1	V
Supply Current @ 10% Duty Cycle in Tx Mode	~ 107	mA
Supply Current @ 90% Duty Cycle in Rx Mode	~ 90	mA
Control Voltage OFF / ON	TTL Compatible 0 / 5	V V
Chip Size	5.3 x 5.3	mm

2. Electrical specifications are measured in a text fixture

Test fixture data in Rx mode (Tx/Rx Control = 0V); Duty cycle = 90%:

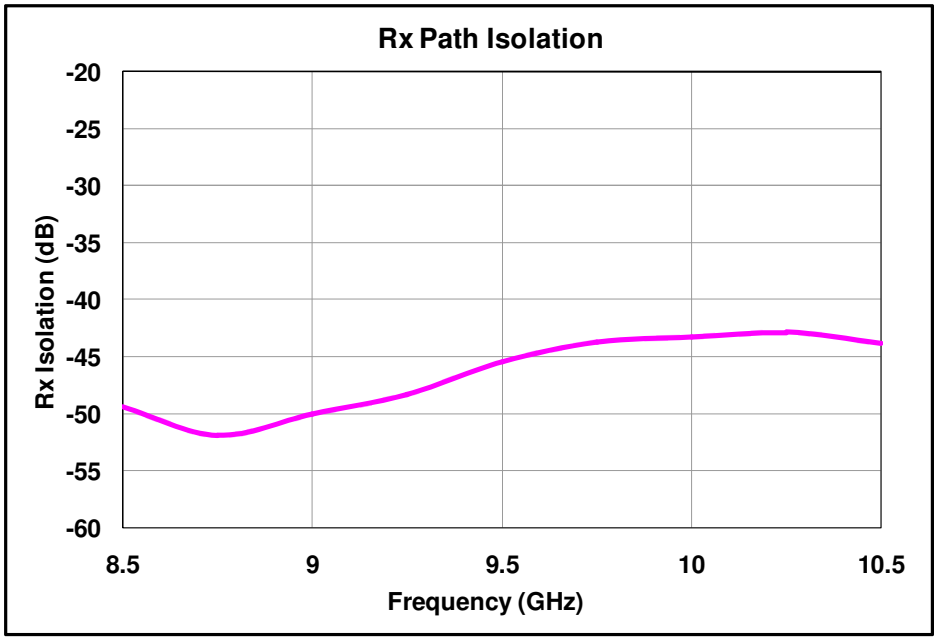
VDDA1 = VDDA2 = 5V ; Total Current = 90mA, T_A = 25 °C

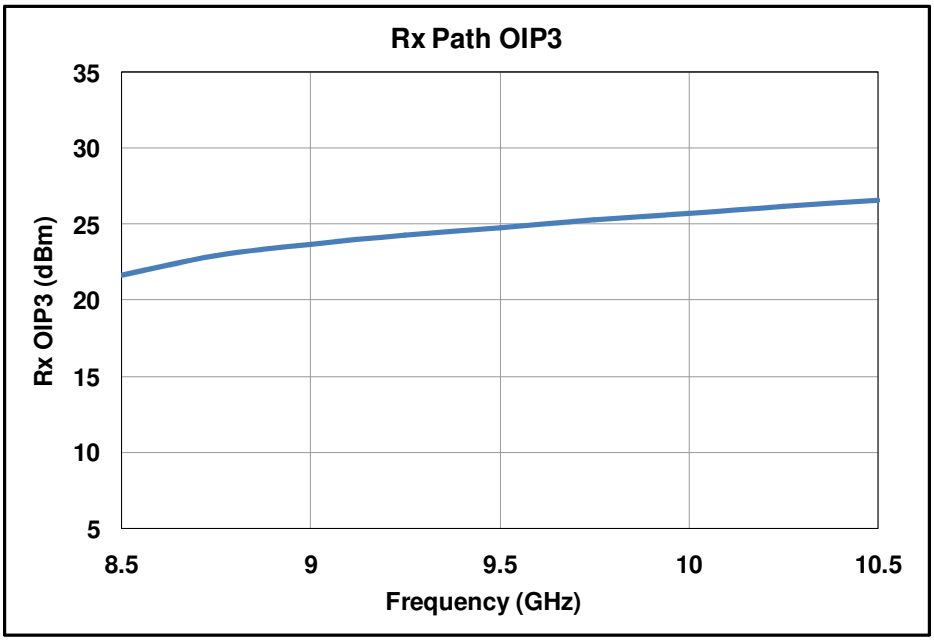




Test fixture data in Rx mode (Tx/Rx Control = 0V); Duty cycle = 90%:

VDDA1 = VDDA2 = 5V ; Total Current = 90mA, T_A = 25 °C





Test fixture data in Rx mode (Tx/Rx Control = 0V); Duty cycle = 90%:

VDDA1 = VDDA2 = 5V ; Total Current = 90mA, T_A = 25 °C

6 Bit Digital Phase Shifter Performance (only prime states):

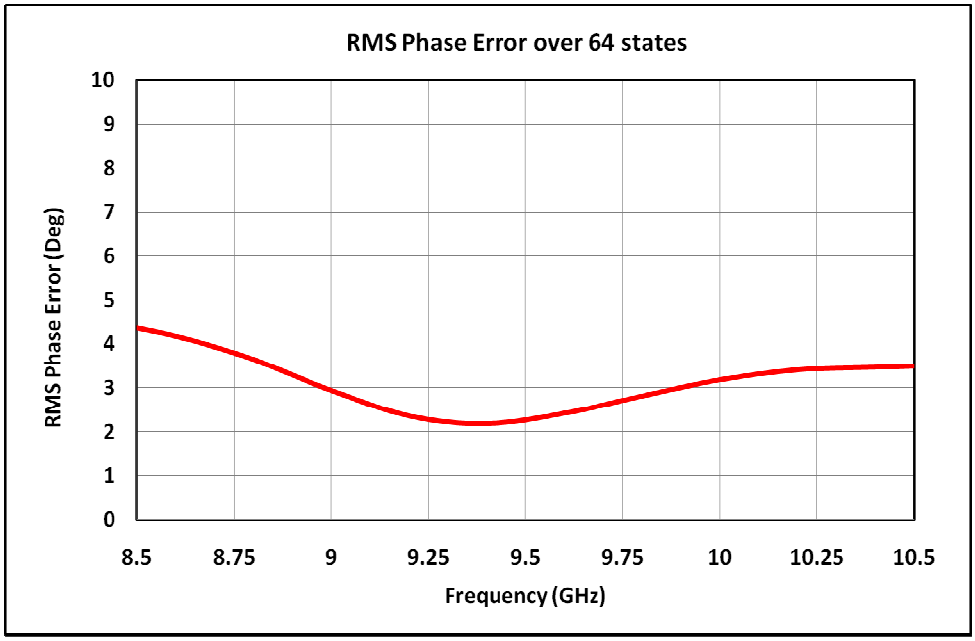
Bit / State (Degree)	Frequency (GHz)		
	9	**9.5**	**10**
5.625 (P0)	6.2	6.4	6.8
11.25 (P1)	12.1	12.3	12.8
22.5 (P2)	20.5	20.6	20.1
45 (P3)	46.3	45	45.5
90 (P4)	90.6	88.5	88.9
180 (P5)	176.3	178.5	179.3

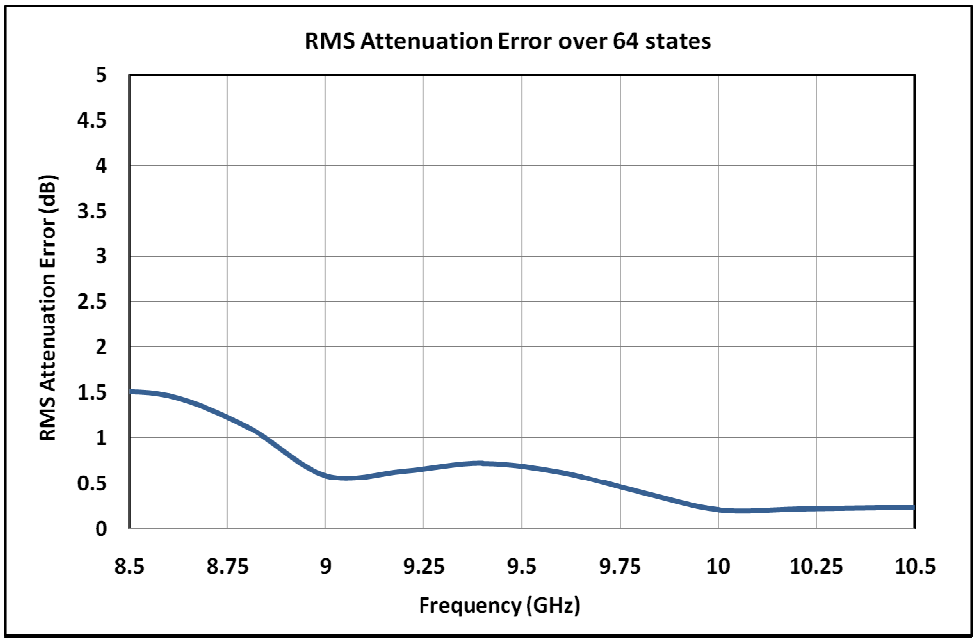
6 Bit Digital Attenuator Performance (only prime states):

Bit / State (dB)	Frequency (GHz)		
	9	**9.5**	**10**
0.5 (A0)	0.43	0.42	0.44
1 (A1)	0.92	0.93	0.95
2 (A2)	2.1	2.05	2.14
4 (A3)	4.02	3.95	4.12
8 (A4)	7.8	8.15	8.2
16 (A5)	16.05	16.75	16.3

Test fixture data in Rx mode (Tx/Rx Control = 0V); Duty cycle = 90%:

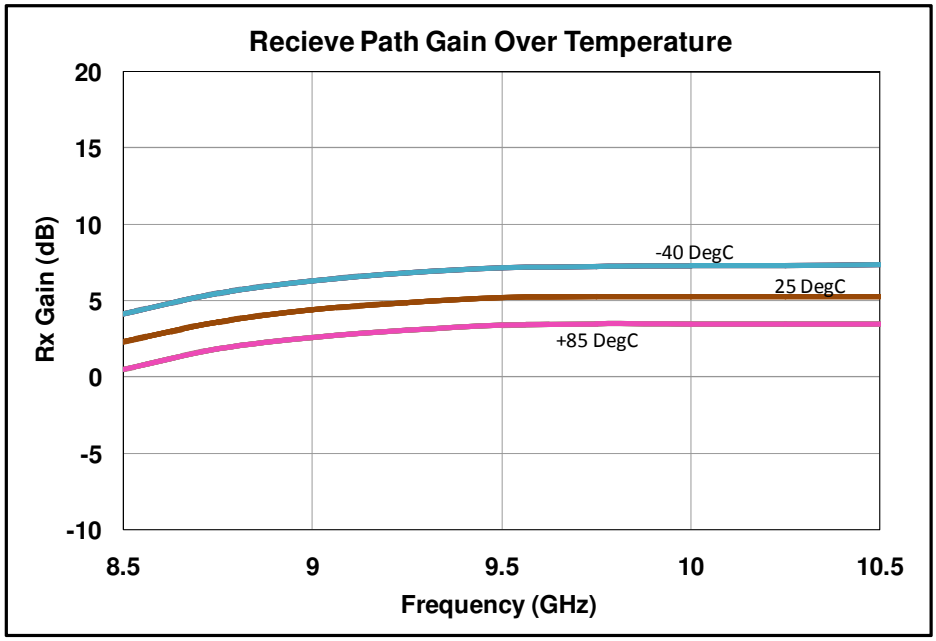
VDDA1 = VDDA2 = 5V ; Total Current = 90mA, T_A = 25 °C

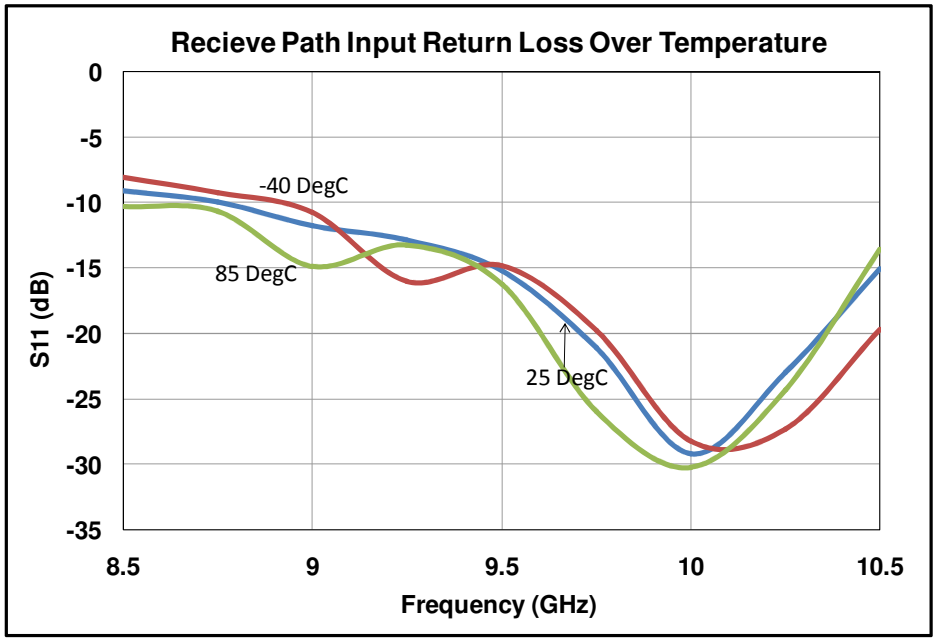




Temperature data in Rx Mode (Tx/Rx Control = 0V); Duty cycle = 90%:

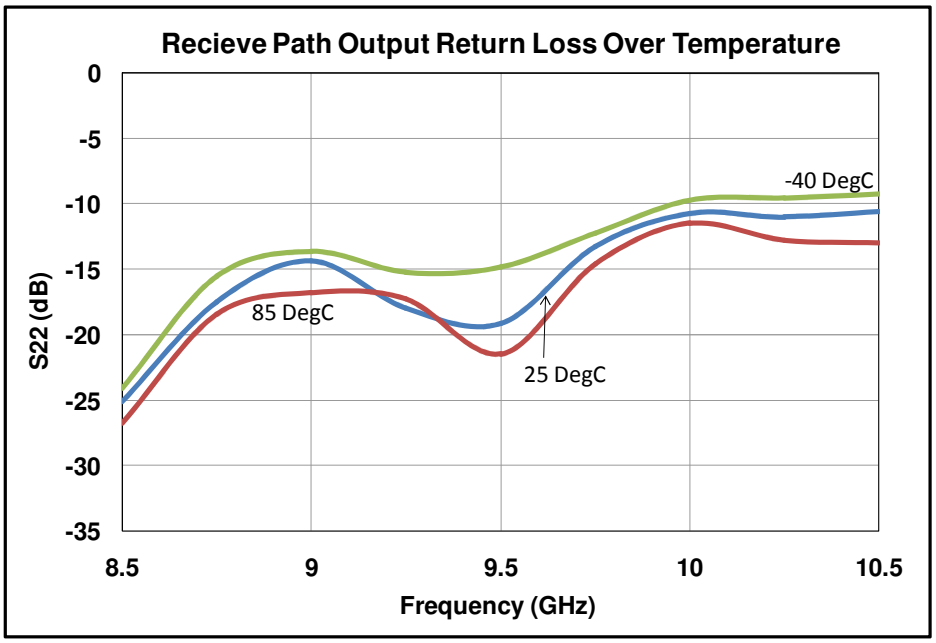
VDDA1 = VDDA2 = 5V ; Total Current = 90mA, T_A = 25 °C





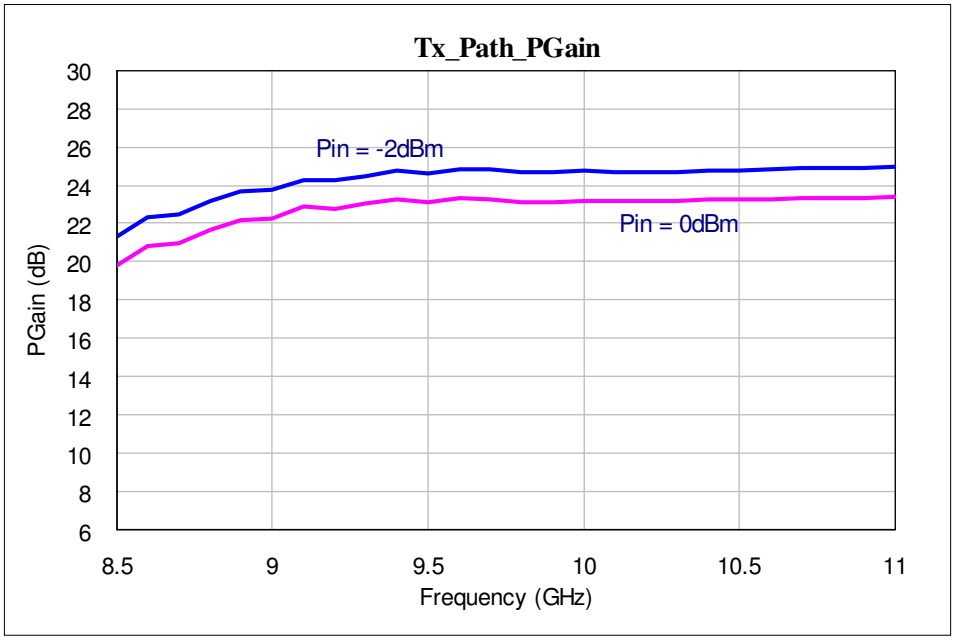
Temperature data in Rx Mode (Tx/Rx Control = 0V); Duty cycle = 90%:

VDDA1 = VDDA2 = 5V ; Total Current = 90mA, T_A = 25 °C

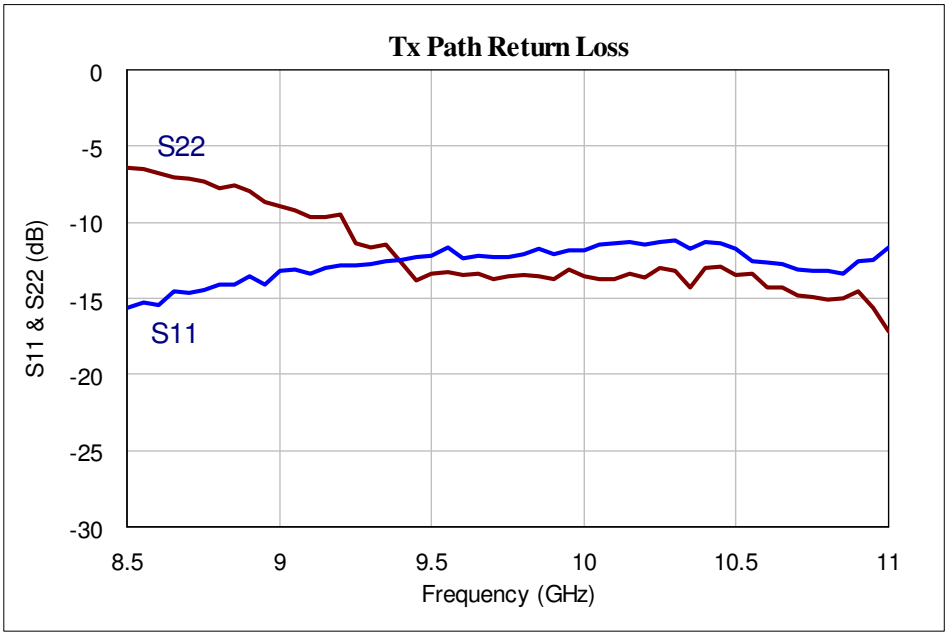


Test fixture data in Tx mode (Tx/Rx Control = 3.3V); Duty cycle = 10%:

VDDA1 = VDDA2 = VDMPA = 5V ; VGMPA = -1V ; Total Current = 107mA, T_A = 25 °C

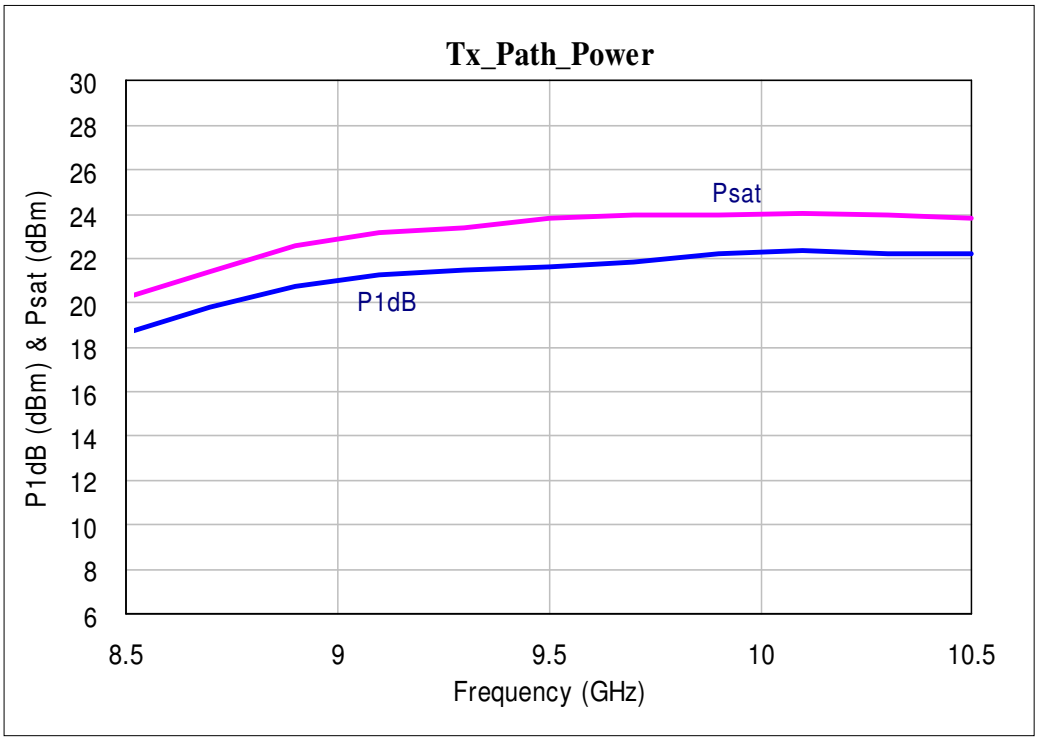


Tx Path Gain over Input Power



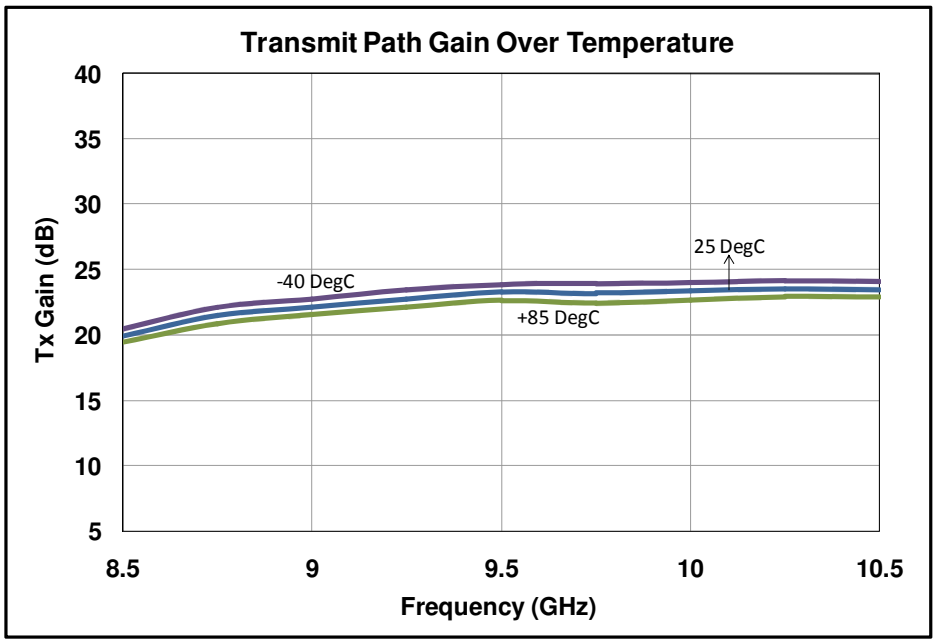
Test fixture data in Tx mode (Tx/Rx Control = 3.3V); Duty cycle = 10%:

VDDA1 = VDDA2 = VDMPA = 5V ; VGMPA = -1V ; Total Current = 107mA, T_A = 25 °C

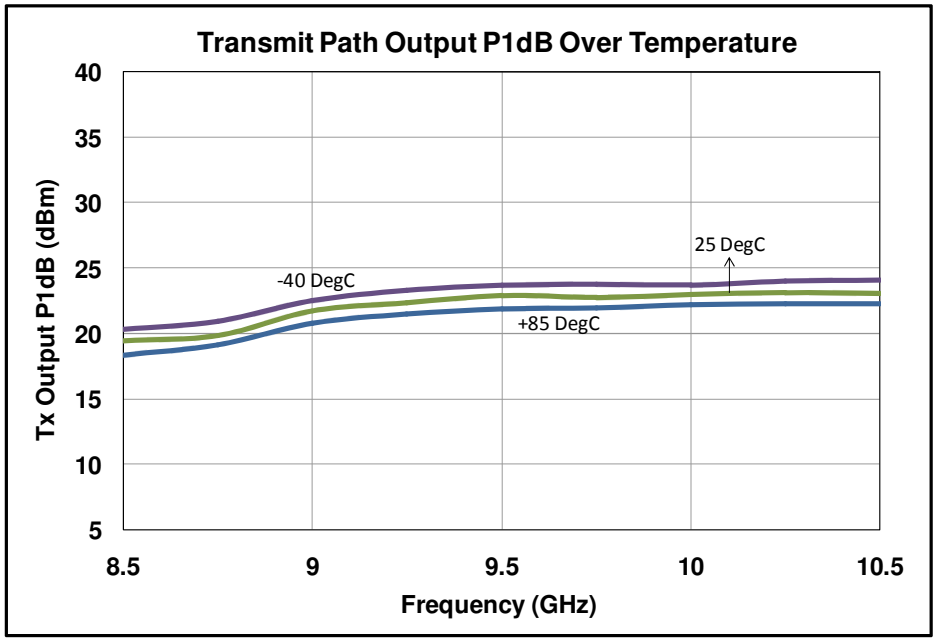


Temperature data in Tx mode (Tx/Rx Control = 3.3V); Duty cycle = 10%:

VDDA1 = VDDA2 = VDMPA = 5V ; VGMPA = -1V ; Total Current = 107mA, T_A = 25 °C

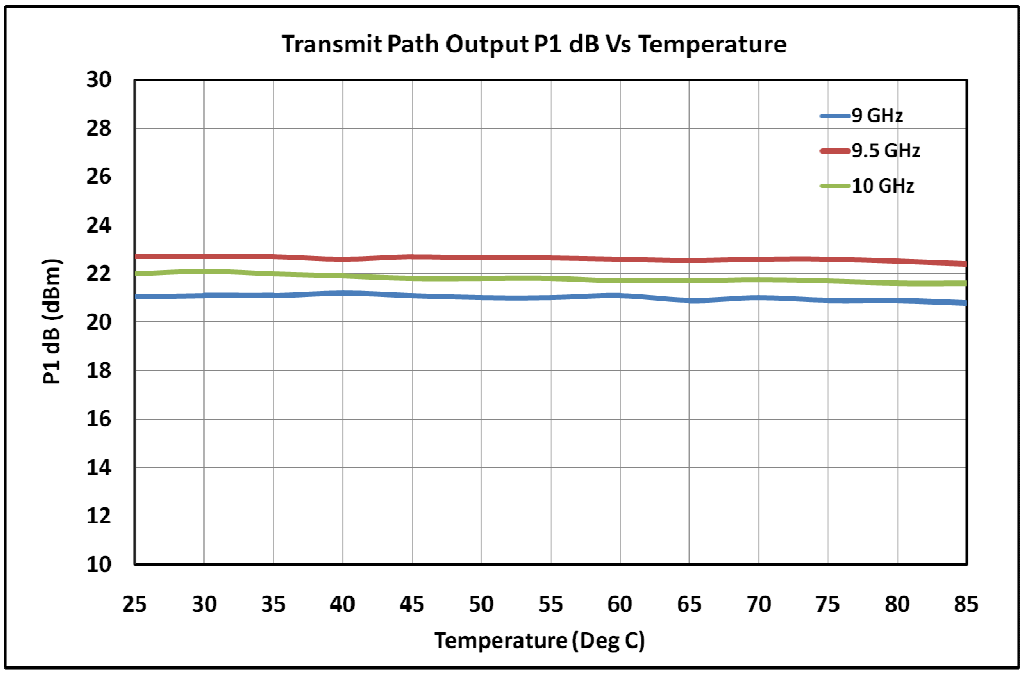


Tx Gain over Temperature @ Pin = 0dBm

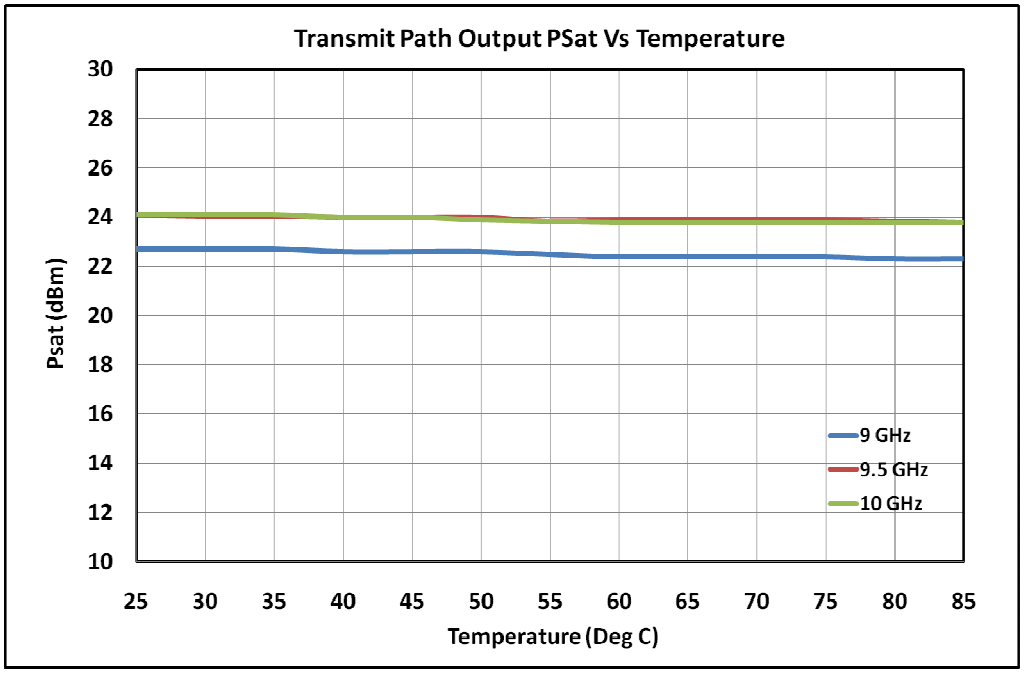


Temperature data in Tx mode (Tx/Rx Control = 3.3V); Duty cycle = 10%:

VDDA1 = VDDA2 = VDMPA = 5V ; VGMPA = -1V ; Total Current = 107mA, T_A = 25 °C



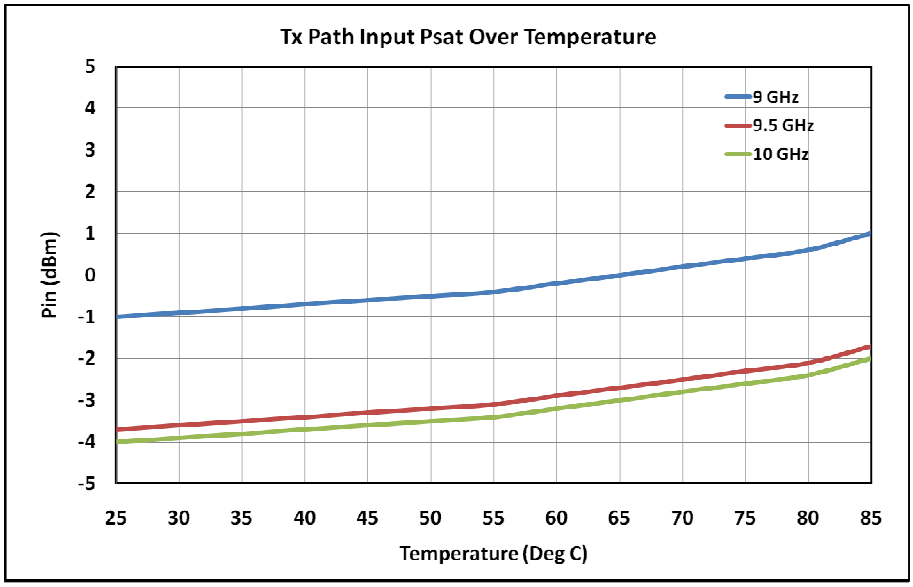
Tx Path Output P1dB plotted with Temperature on X-axis



Tx Path Output Psat plotted with Temperature on X-axis

Temperature data in Tx mode (Tx/Rx Control = 3.3V); Duty cycle = 10%:

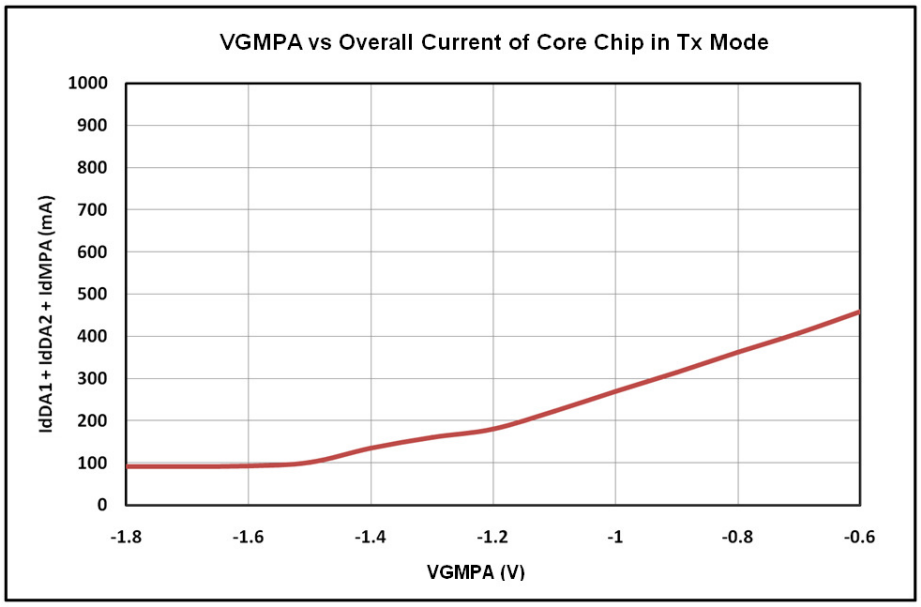
VDDA1 = VDDA2 = VDMPA = 5V ; VGMPA = -1V ; Total Current = 107mA, T_A = 25 °C



Tx Path Input Power of Core Chip Corresponding to Saturated Output Power Plotted with Temperature on X-axis

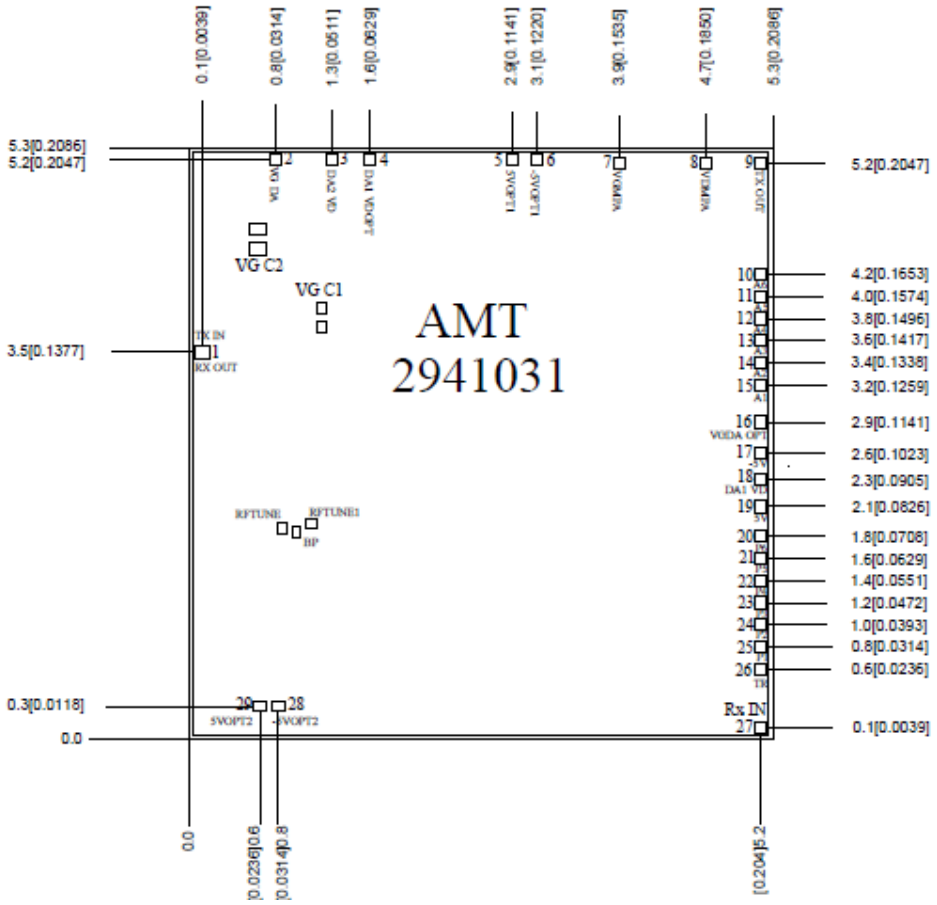
Test fixture data in Tx mode (Tx/Rx Control = 3.3V); CW mode

VDDA1 = VDDA2 = VDMPA = 5V, T_A = 25 °C



Overall Quiescent Current variation of core chip in Tx mode by varying gate voltage (VGMPA)

Bond Pad Locations:



Units: Millimetres [Inches]

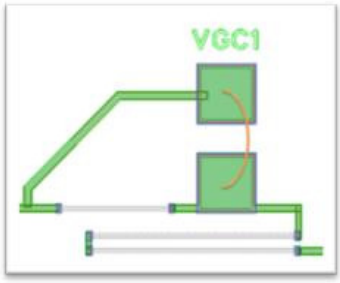
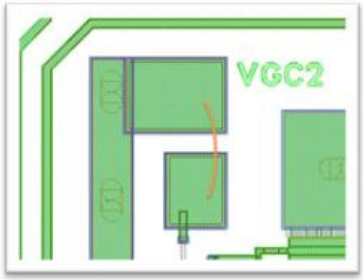
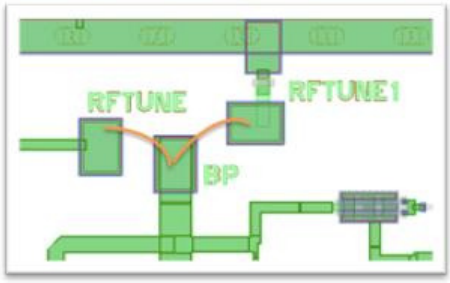
All RF and DC bond pads are 100µm x 100µm

Bond Pad Details and Connections:

PAD NO	PAD LABLE	PAD DESCRIPTION / CONNECTION
1	TXIN / RXOUT	To be connected to 100pF SLC (Decoupling capacitor) to RF track (two 1 mil bond wires)
3	DA2 VD	To be connected through 100pF SLC then 0.1uF to +5V supply (two 1 mil bond wires)
4	DA1 VD OPT	To be connected to 50 ohm Thin film resistor then 100pF Single Layer bypass Capacitor (two 1 mil bond wires)
7	VG MPA	To be connected through 100pF SLC then 1uF to -1V (Two 1 mil bond wires) in case of Drain Pulsing Core Chip MPA. To be connected through 100pF SLC to -1V (Two 1 mil bond wires) in case of Gate Pulsing Core Chip MPA.
8	VD MPA	To be connected through 100pF SLC then 1kpF to +5V supply (two 1 mil bond wires) in case of Drain Pulsing Core Chip MPA. To be connected through 100pF SLC then 1uF to +5V supply (two 1 mil bond wires) in case of Gate Pulsing Core Chip MPA.
9	TX OUT	To be connected to RF track (two 1 mil bond wires)
10-15	A6 – A1	Attenuator controls (3.3V to 5V) have to be connected to ATTN control signal tracks (Single 1 mil bond wires)
18	DA1 VD	To be connected through 100pF SLC then 0.1uF to +5V (Single 1 mil bond wires)
20-25	P6-P1	Phase Shifter controls (3.3V to 5V) have to be connected to PS control signal tracks (Single 1 mil bond wires)
26	TR	Switch control (3.3V to 5V) have to be connected to T/R switch control signal track (Single 1 mil bond wires)
27	RX IN	To be connected to RF track (two 1 mil bond wires) *100pF SLC (Decoupling capacitor) required if next stage does not have decoupling capacitor.*
2	VG DA	No Connection
16	VG DA OPT	
Supply Pads		
5	5V OPT1	**Three Optional Pads for +5V Control Supply.** +5V supply is to be connected to any one of the three pads through 100pF SLC then 0.1uF (or 1uF) to +5V supply (two 1 mil bond wires). The other two remaining pads are “NC”.
19	5V	
29	5V OPT2	
6	-5V OPT1	**Three Optional Pads for -5V Control Supply.** -5V supply is to be connected to any one of the three pads through 100pF SLC then 0.1uF (or 1uF) to -5V supply (two 1 mil bond wires). The other two remaining pads are “NC”.
17	-5V	
28	-5V OPT2	

On Chip Tuning Pad Details and Connections

OPTIONAL USE – TO BE USED ONLY AS PER SYSTEM SPECIFIC REQUIREMENT

VGC1	There are two pads shown at the location marked VGC1. By shorting these two on chip Bond Pads (using single 1 mil bond wire), the gain across Tx path and Rx path reduces by 2dB and overall current of the core chip reduces by 34mA.	
VGC2	There are two pads shown at the location marked VGC2. By shorting these two on chip Bond Pads (using single 1 mil bond wire), the gain across Tx path and Rx path increases by 1dB and overall current of the core chip increases by 18mA.	
RFTUNE, RFTUNE1, BP	These three Pads are to be shorted (using single 1 mil bond wire), to further improve return loss at the common port (Txin/Rxout) of the core chip.	

Operation of Core Chip in Tx Mode / Rx Mode:

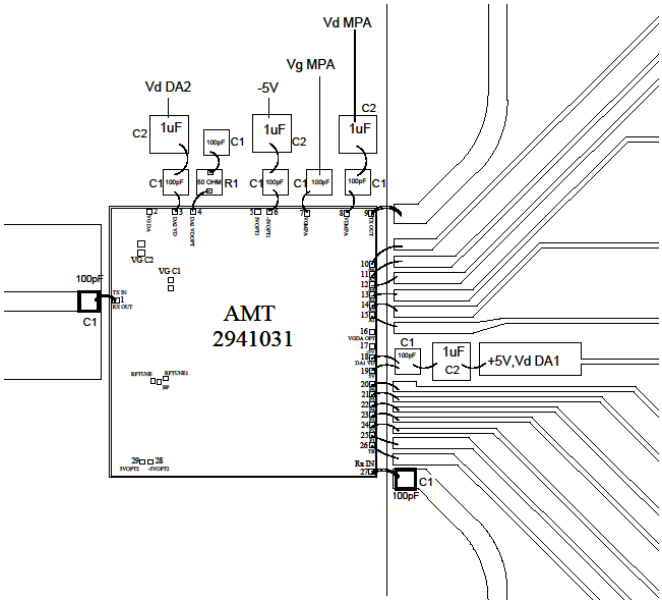
Core Chip (AMT2941031) can be operated in Tx Mode or Rx Mode by applying PRT to Pad No. 26 '**T/R Switch Control**' and simultaneously switching MPA of the core chip to ON state or OFF state by pulsing 'VGMPA' or 'VDMPA' across Tx Path respectively.

The MPA of the core chip is 'ON' when core chip is in TX Mode and it is 'OFF' when core chip is in Rx Mode.

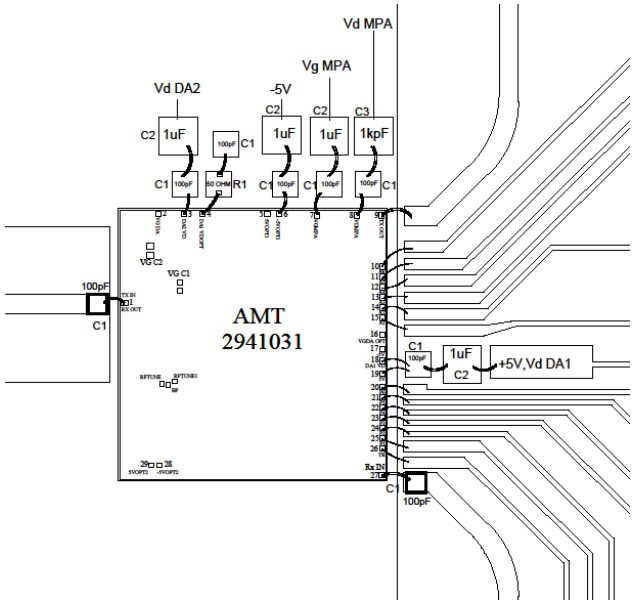
Recommended Assembly Diagrams:

Two separate assembly drawings are recommended for pulsing VGMPA and VDMPA of the core chip as given below. These two assemblies given below can also be referred to operate MPA of the core chip in continuous mode.

a. Recommended assembly diagram for Pulsing VGMPA of the core chip



b. Recommended assembly diagram for Pulsing VDMPA of the core chip



Note:

1. Input and output 50 ohm lines are on 5 mil substrate.
2. Use high thermal conductive material for die mounting in order to achieve higher MTBF of the device.
3. **Die attach:** For Epoxy attachment, use of a two-component conductive epoxy is recommended. An epoxy fillet should be visible around the total die periphery. If Eutectic attachment is preferred, use of fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.
4. **Wire bonding:** For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200µm length of wedge bonds is advised. Single Ball bonds of 250-300µm though acceptable, may cause a deviation in RF performance.

Off Chip Components used while recording Test Fixture Data:

Component	Part Number / Description	Vendor
100pF SLC Capacitor (C1)	D12BV101K5PX/100pF±10%;50V or Equivalent	DLI
1uF MLC Capacitor (C2)	04023C105KAT2A/1uF±10%;25V or Equivalent	AVX Corporation
1kpF MLC Capacitor (C3)	04023C102KAT2A/1kpF±10%;25V or Equivalent	AVX Corporation
1674011 330ohm Multi-Tap GaAs MMIC Resistor (R1)	ASTRA1674011/330ohm±5%;10V or Equivalent (50ohm resistance is derived from multi tap 330ohm)	ASTRA

Truth Table for 6 Bit Digital Attenuator:

State	Attenuation (dB)	TTL Control (1 = 3.3 to 5 V, 0 = 0 to 0.2 V)					
		A5 (16)	A4 (8)	A3(4)	A2 (2)	A1(1)	A0 (0.5)
0	0	0	0	0	0	0	0
1	0.5	0	0	0	0	0	1
2	1	0	0	0	0	1	0
4	2	0	0	0	1	0	0
8	4	0	0	1	0	0	0
16	8	0	1	0	0	0	0
32	16	1	0	0	0	0	0
63	31.5	1	1	1	1	1	1

Truth Table for 6 Bit Digital Phase Shifter:

State	Phase (Deg)	TTL Control (1 = 3.3 to 5 V, 0 = 0 to 0.2 V)					
		P5 (180)	P4 (90)	P3(45)	P2 (22.5)	P1(11.25)	P0 (5.625)
0	0	0	0	0	0	0	0
1	5.625	0	0	0	0	0	1
2	11.25	0	0	0	0	1	0
4	22.5	0	0	0	1	0	0
8	45	0	0	1	0	0	0
16	90	0	1	0	0	0	0
32	180	1	0	0	0	0	0
63	354.375	1	1	1	1	1	1

ATTENTION
OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice. Please download and refer to datasheet from website before using the product.