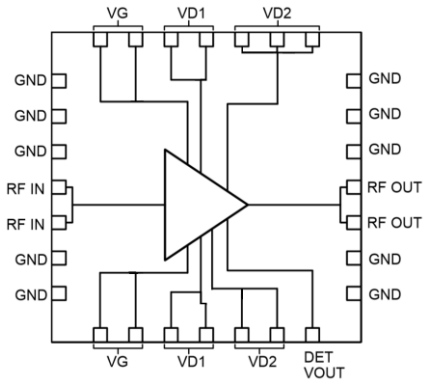
# 8.5 – 10GHz 12 Watt Power Amplifier

## Features

- **Frequency Range : 8.5 – 10GHz**
- **12W Psat**
- **23dB Small Signal Gain**
- **32% PAE**
- **High IP3**
- **Dual bias operation**
- **DC decoupled input and output**
- **On Chip Power Detector**
- **InGaAs pHEMT Technology**
- **7mm SQ. QFN Package**

**Functional Diagram**




## Typical Applications

- **RADAR**
- **Military & space**
- **LMDS, VSAT**

## Description

The AMT2144116P7 is a X-band Power amplifier with 12Watt Saturated Output Power. The PA uses 2 stages of amplification and operates over 8.5 – 10GHz frequency range. It features 23dB of Small Signal Gain. It has a high IP3 of 48dBm and 32% PAE. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage. It is fabricated using a reliable InGaAs pHEMT technology.

## Absolute Maximum Ratings (Not Simultaneous) (1)

| Parameter | Absolute Maximum | Units |
|---|---|---|
| Drain bias voltage (Vd)(2) | +8.5 | volts |
| Drain current ($Id_{Peak}$) at Vd=8V(2) | 6 | A |
| Gate Voltage | -2.2 < Vg < -0.6 | V |
| RF input power (RFin at Vd=8V)(2) | 24 | dBm |
| Operating temperature(2) | -50 to +85 | °C |
| Storage Temperature | -65 to +150 | °C |

1. Operation beyond these limits may cause permanent damage to the component.
2. Measured at 20% Pulse Duty Cycle unless otherwise specified.

## Electrical Specifications [1] @ $T_A$ = 25 °C, Vd1 = Vd2 = 8V, Vg1 = Vg2 = -0.85V
## $Z_o$ = 50Ω, Pulse Duty Cycle = 10%

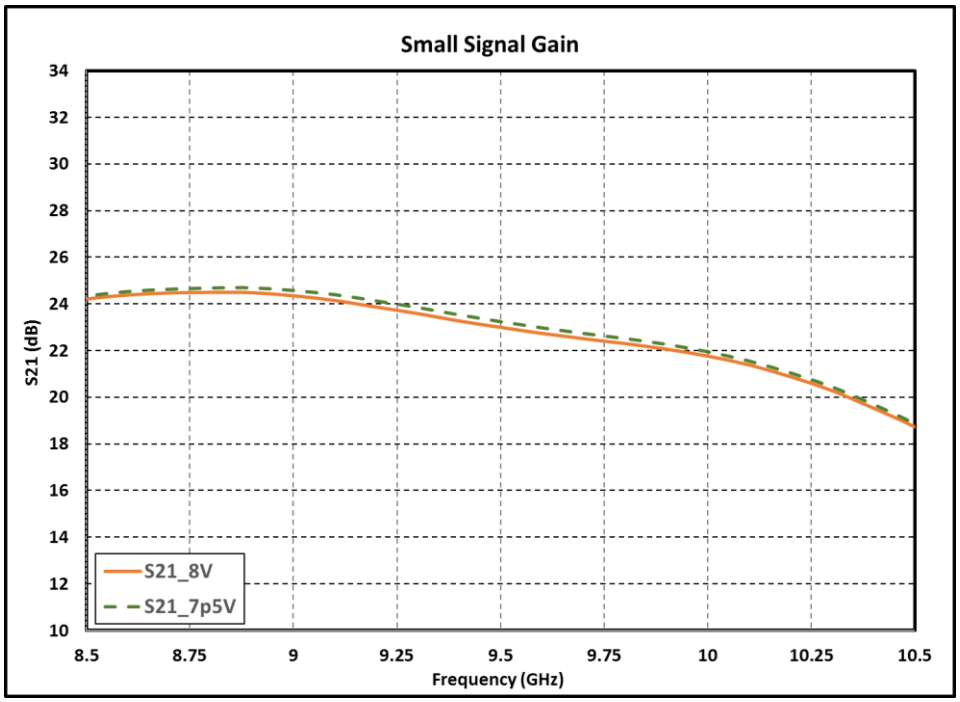
| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Frequency Range | | 8.5 – 10 | | **GHz** |
| Small Signal Gain | 21 | 23 | | dB |
| Gain Flatness | | +/-1.5 | | dB |
| Output Power (P1 dB) | 38.5 | 39.5 | | dBm |
| Input Return Loss | | 9 | | dB |
| Output Return Loss | | 6 | | dB |
| Saturated output power (Psat) | 40 | 40.8 | | dBm |
| Output Third Order Intercept (IP3) | | 48 | | dBm |
| Power Added Efficiency (PAE) | | 32% | | -- |
| Drain Voltage ($V_d$) | | 8 | | V |
| Gate Voltage ($V_g$) | -0.6 | -0.85 | -1.2 | |
| Supply Current($I_{dq}$) | | 2.5 | | A |
| Supply Current($I_{dsat}$) | | 5 | 6 | A |

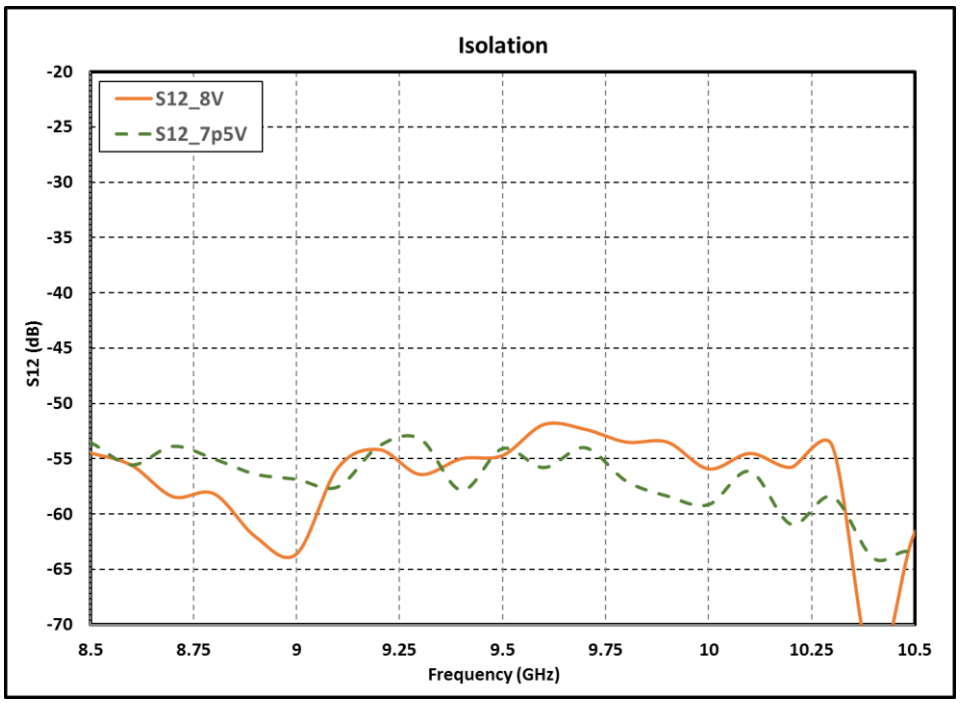
***Note:***

1. Electrical specifications as measured in test fixture.
2. $I_{dsat}$ – Drain Current at Saturated Output Power.

## Test fixture data

*$V_{d1}$ = $V_{d2}$ = $V_d$, $V_{g1}$ = $V_{g2}$ = -0.85V, Total Current (Idq) = 2.5A, $T_A$ = 25 °C, Pulse Duty Cycle = 10%*



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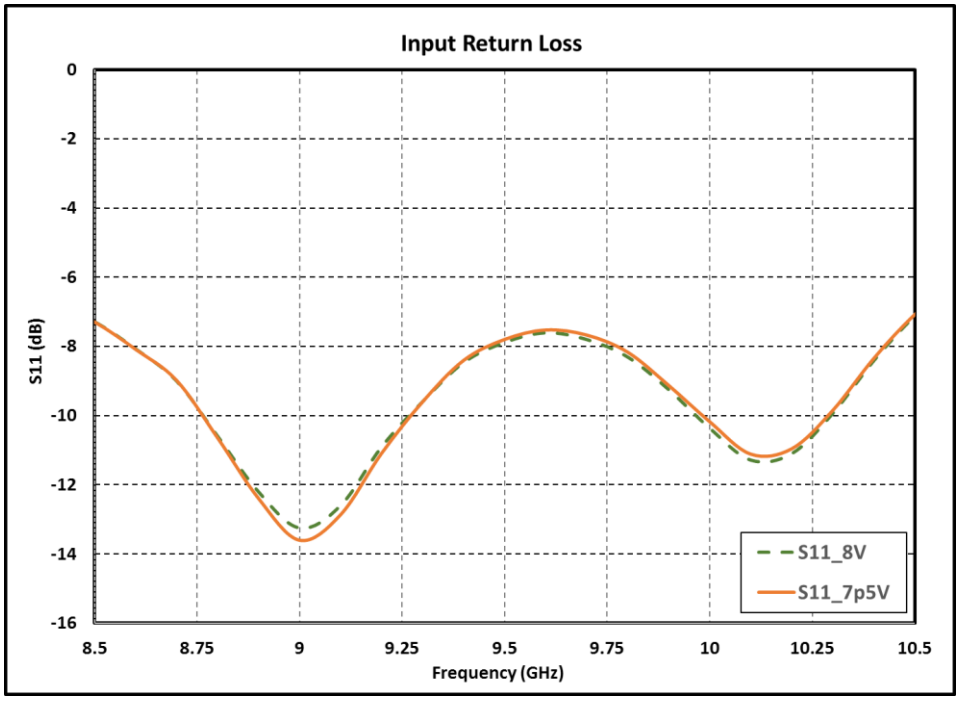


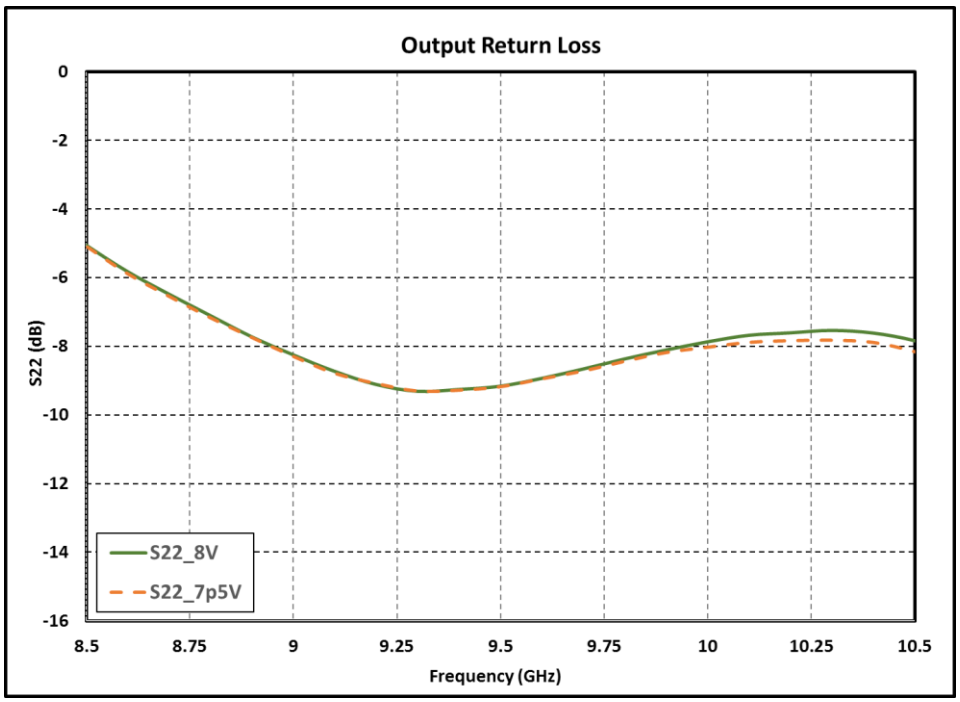

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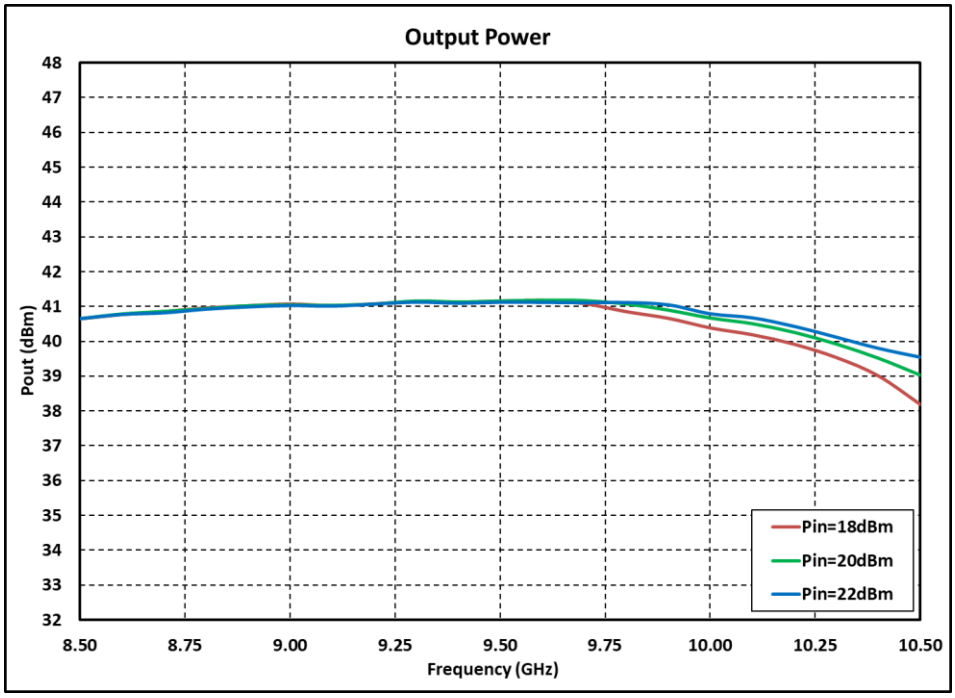


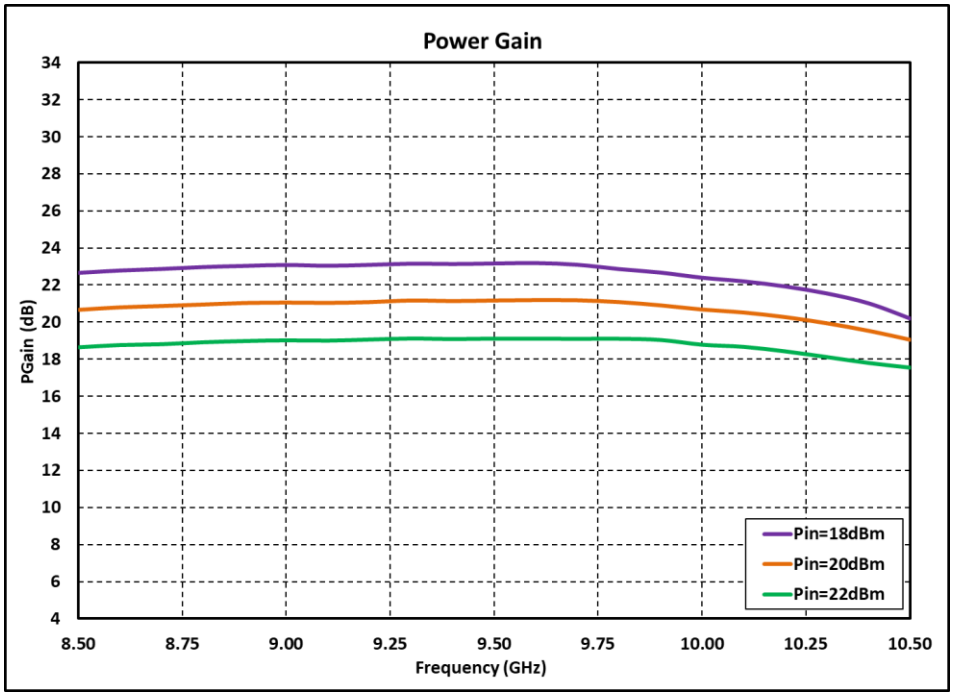

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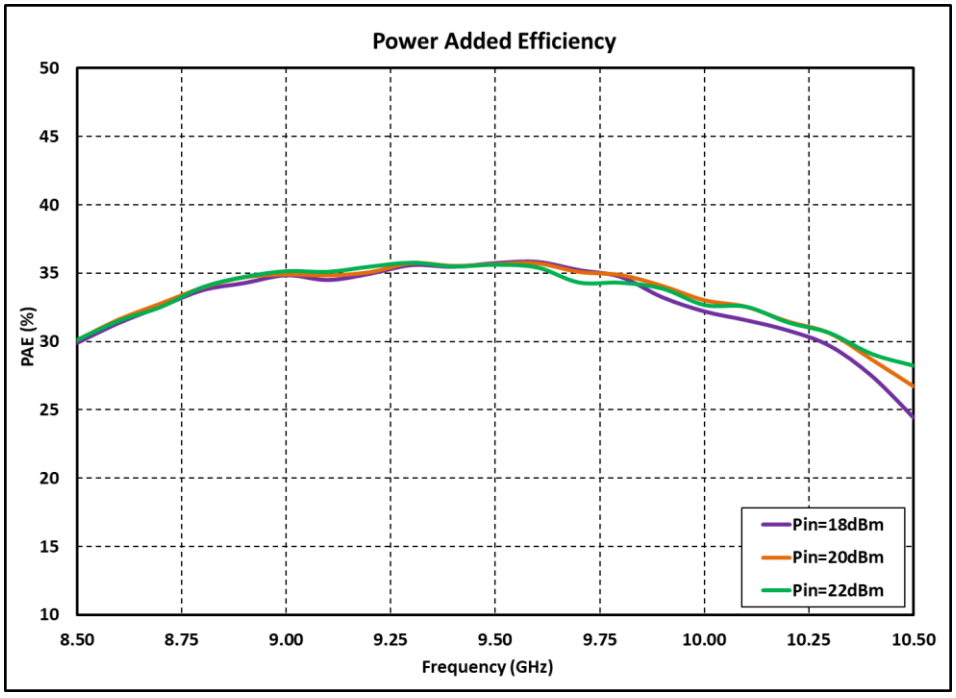


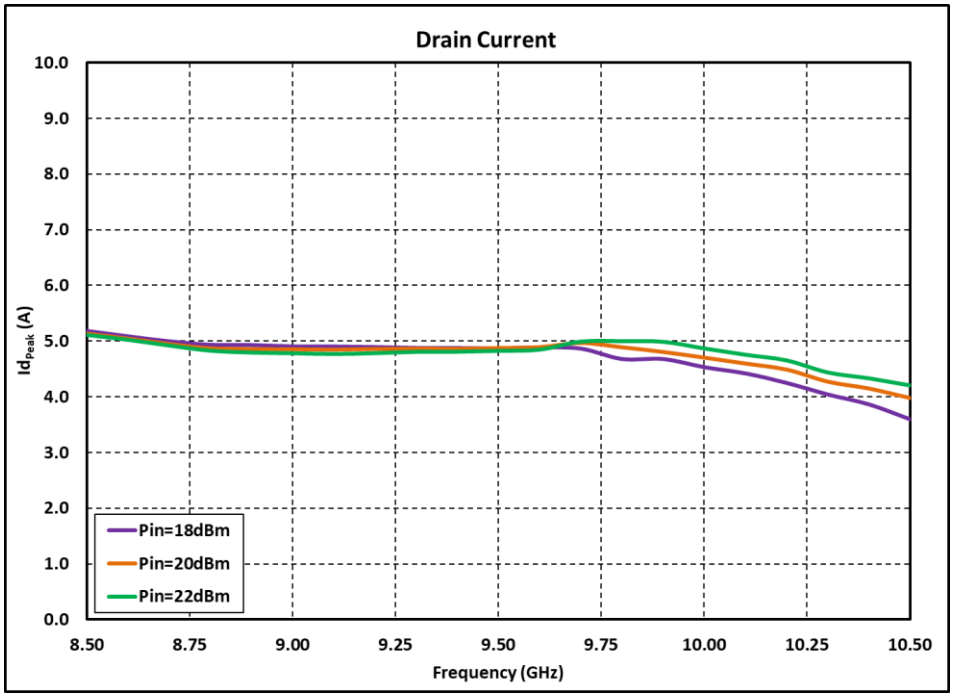

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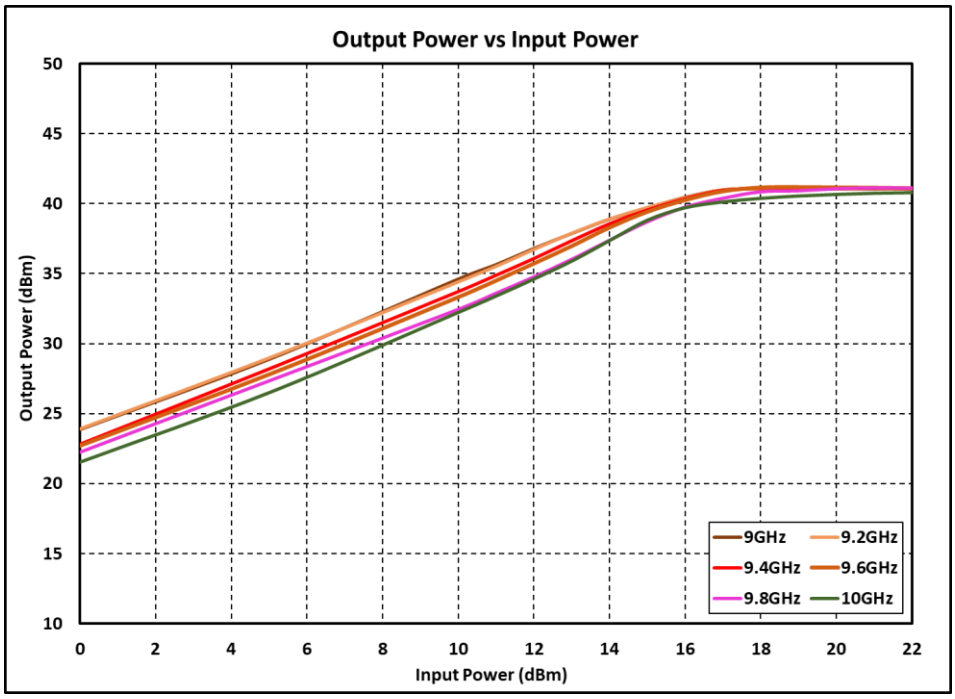


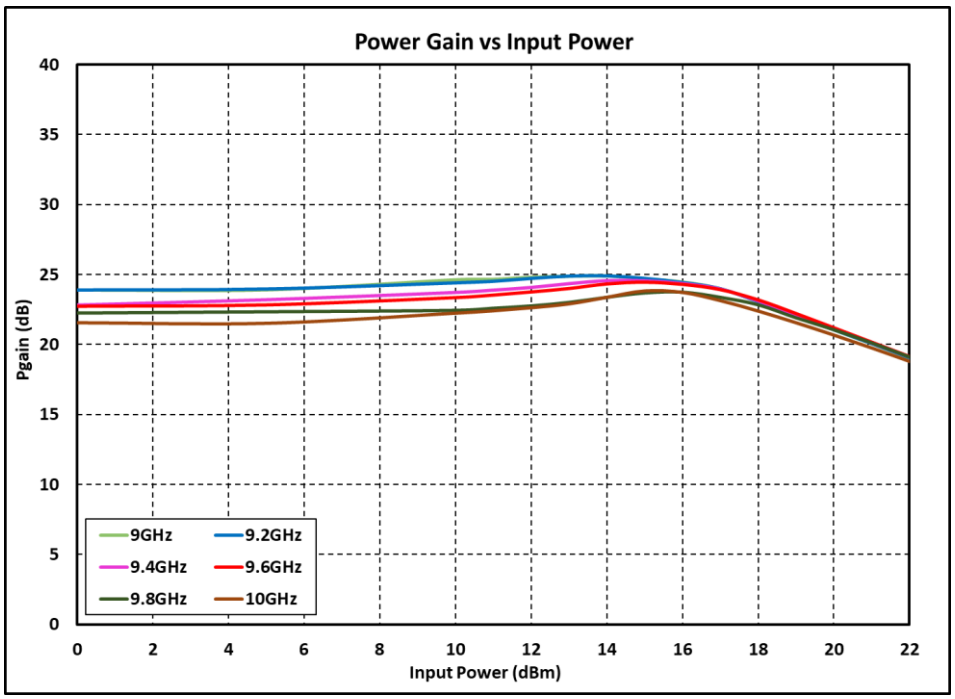

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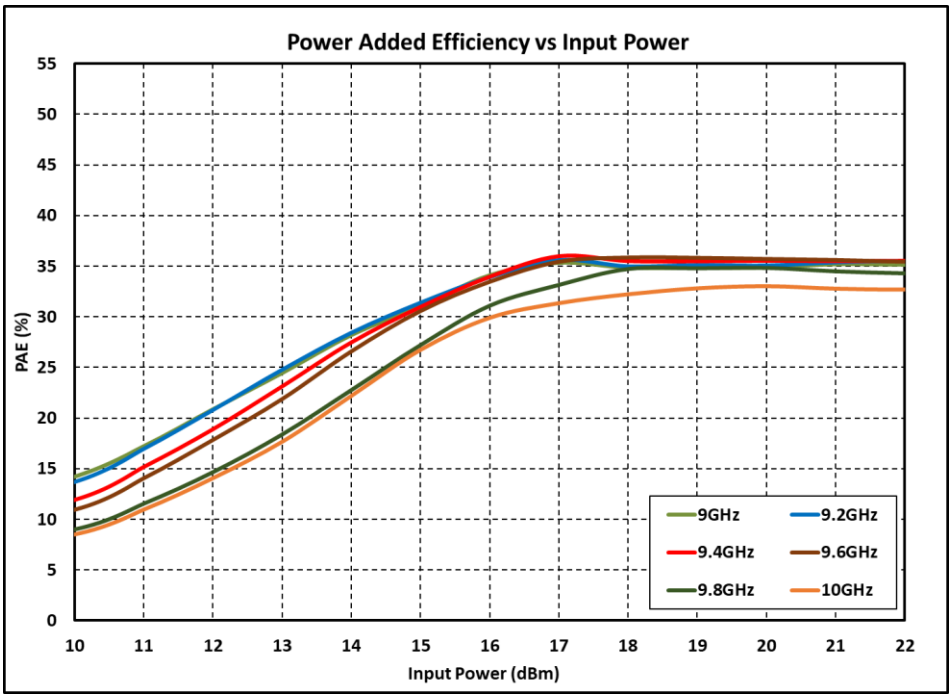


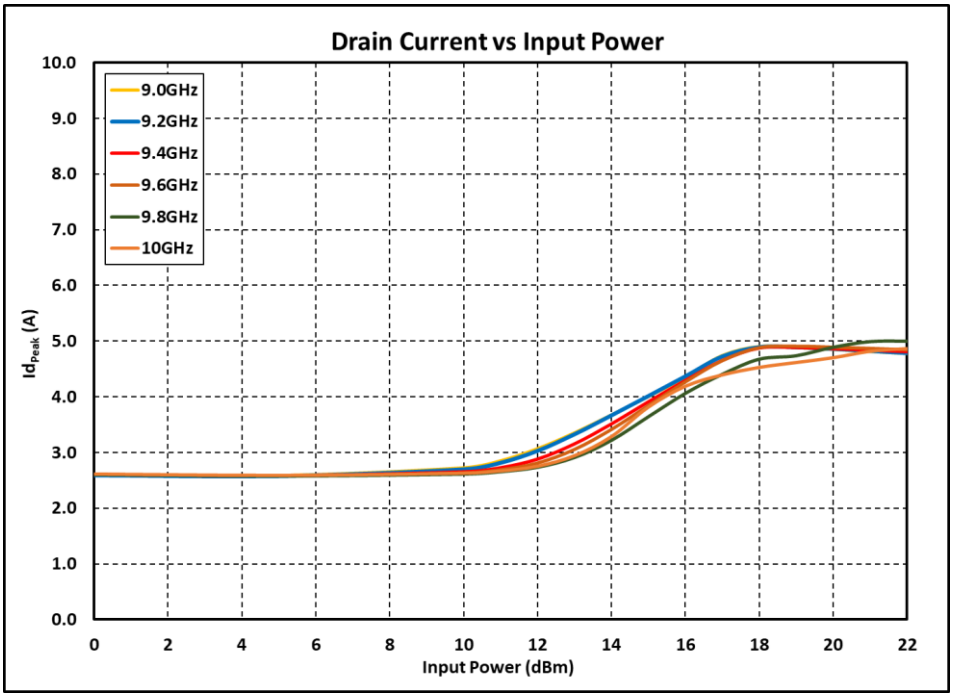

## Test fixture data

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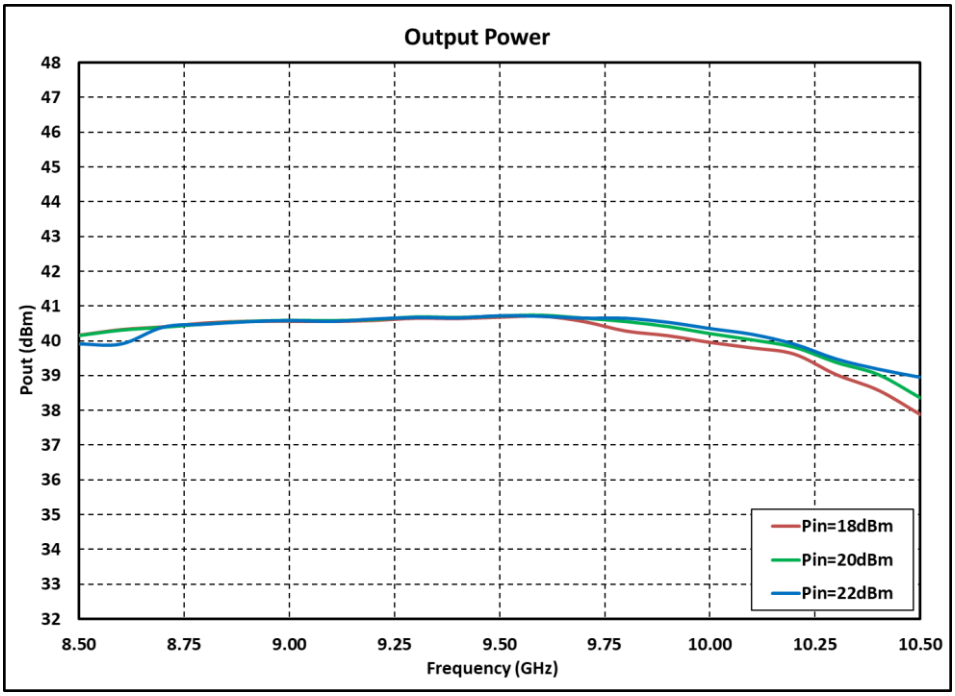


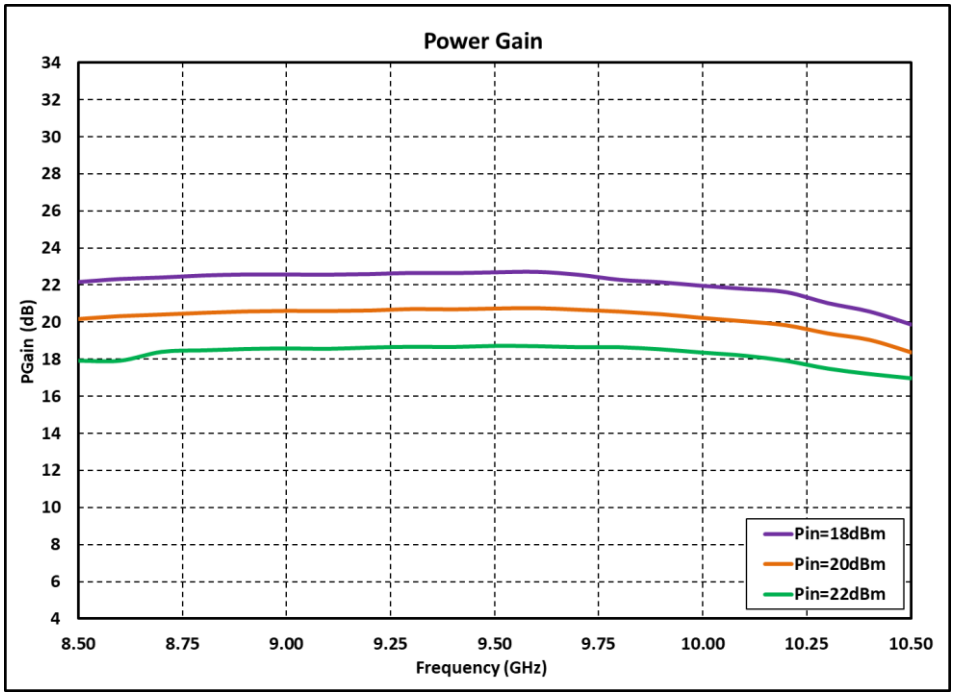

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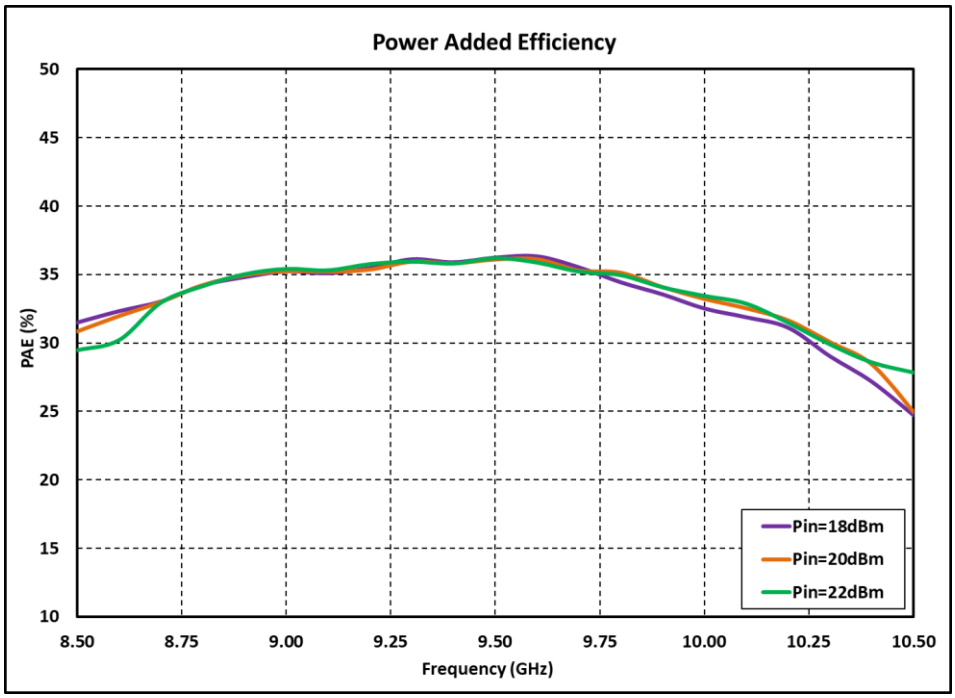


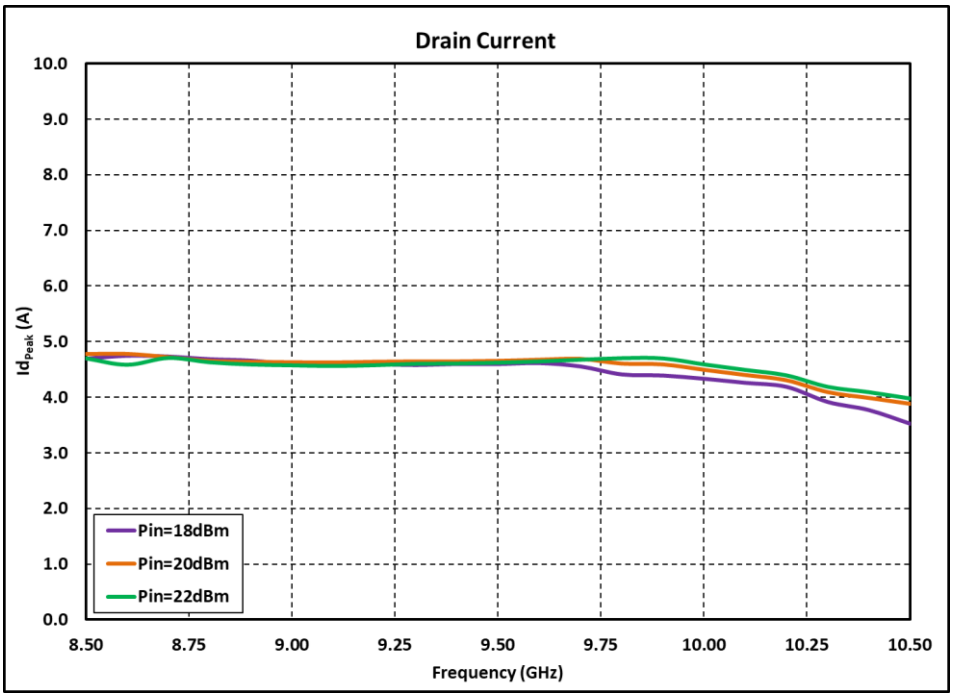

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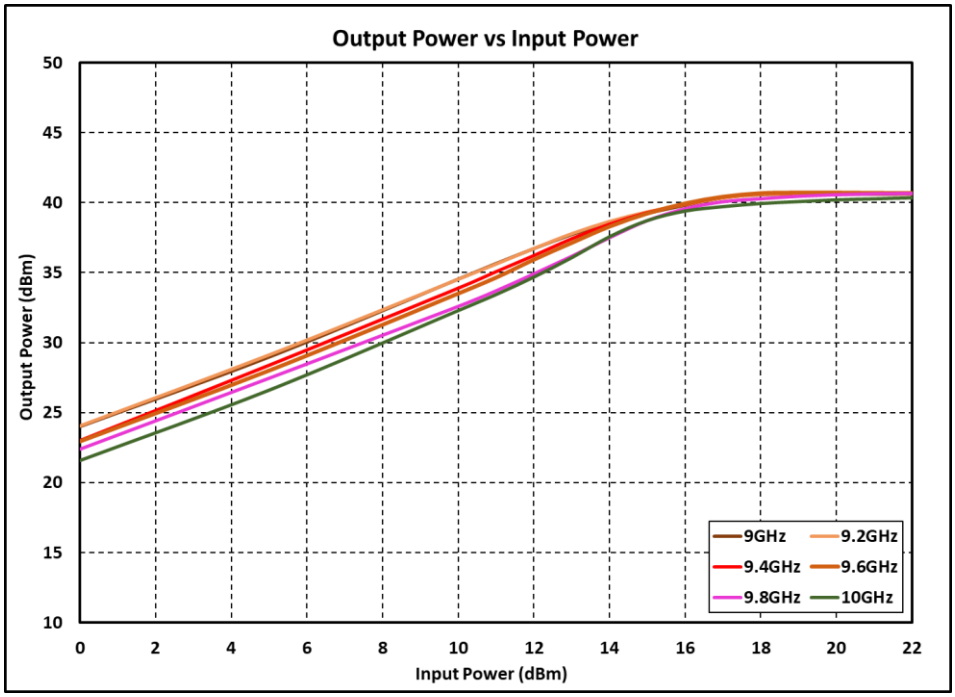


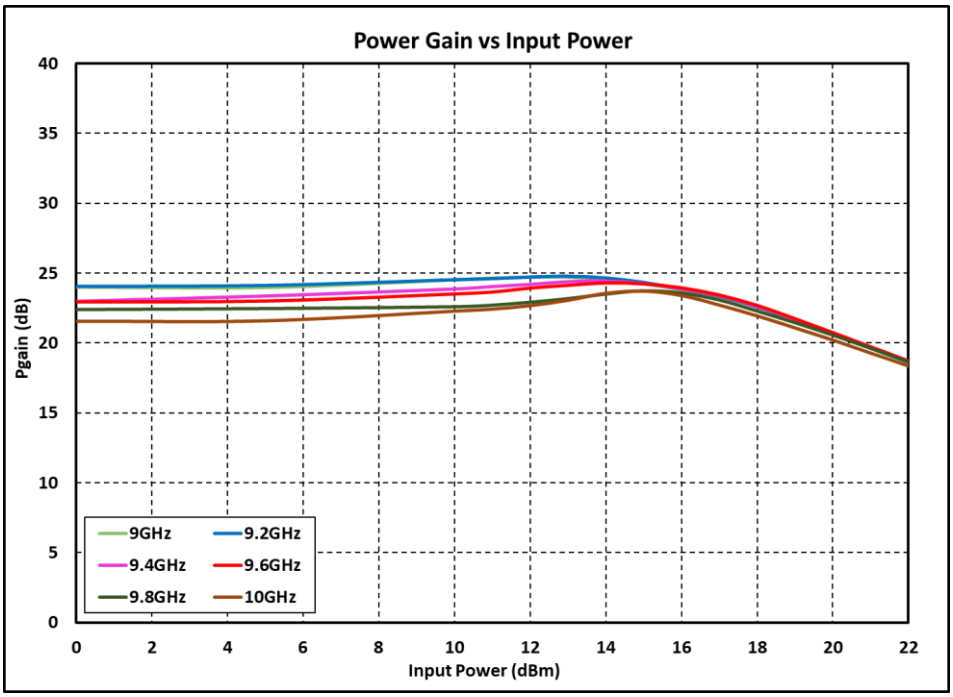

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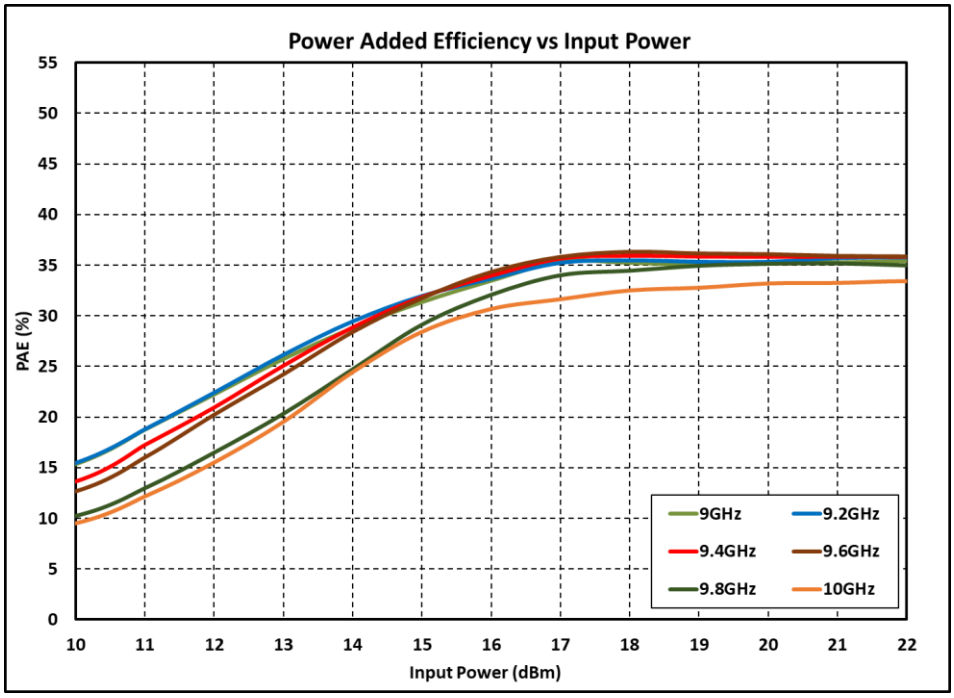
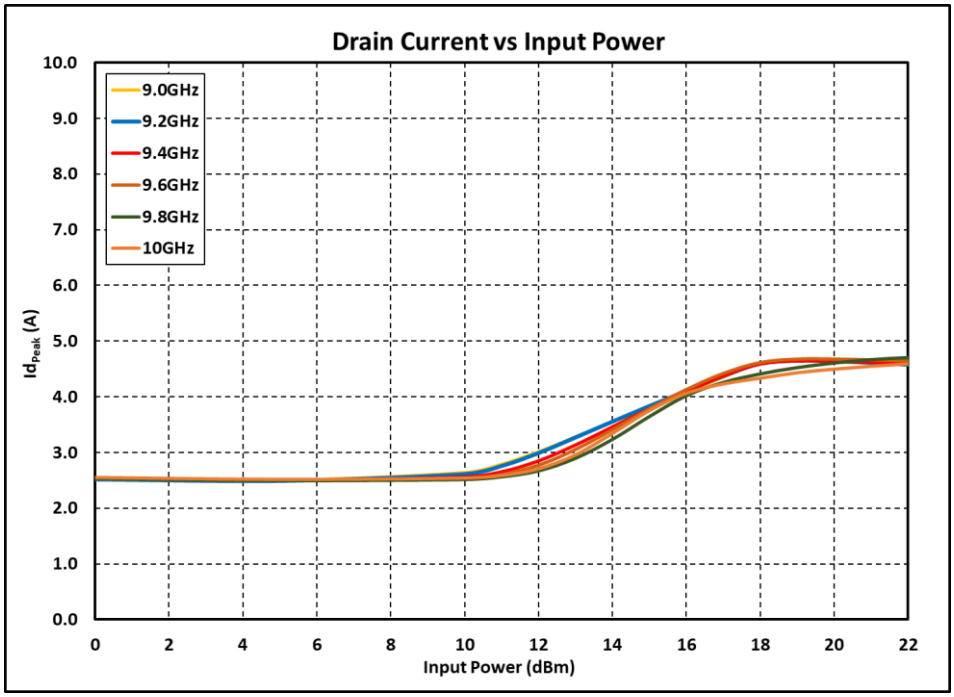


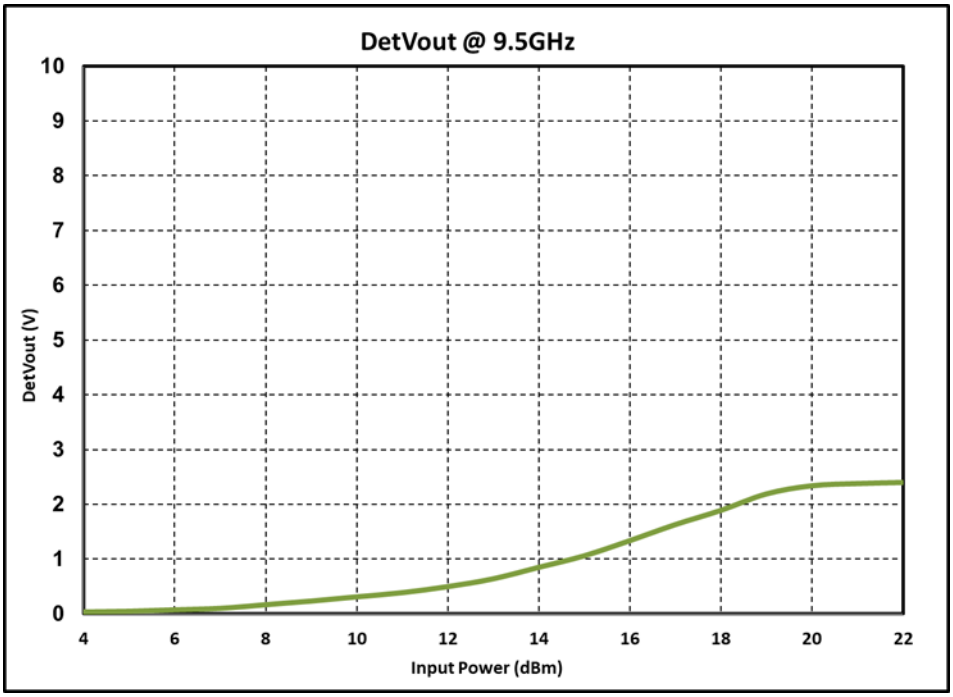
# Power Detector Performance:

## Test fixture data

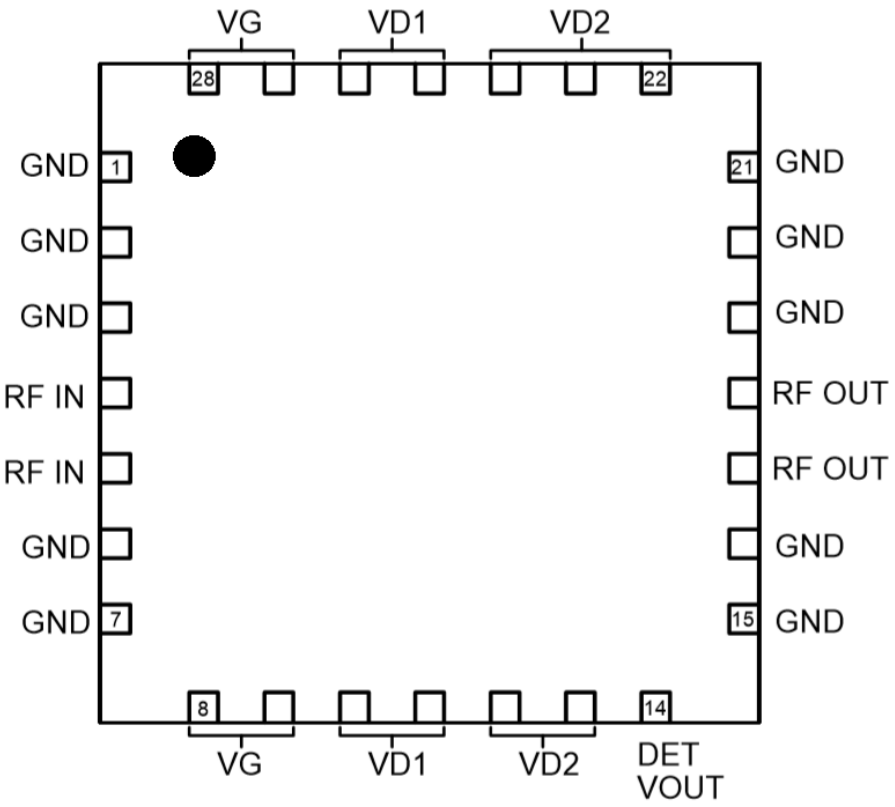
*$V_{d1}$ = $V_{d2}$ = 8V, $V_{g1}$ = $V_{g2}$ = -0.85V, Total Current (Idq) =2.5A, $T_A$ = 25 $^oC$, Pulse Duty Cycle = 10%*

| Pout (dBm) | DetVout @ 9GHz | DetVout @ 9.5GHz | DetVout @ 10GHz |
|---|---|---|---|
| 40.8dBm | 2.2V | 2.4V | 2.3V |
| -30dBm | 0V | 0V | 0V |

**Description:** The Output Voltage of the detector ”DetVout” increases with increase in RF output power of the power amplifier. The output of the detector is tapped from ”DetVout”.
The performance of the detector with respect to variation in the input power of the PA at 9.5GHz is plotted below.



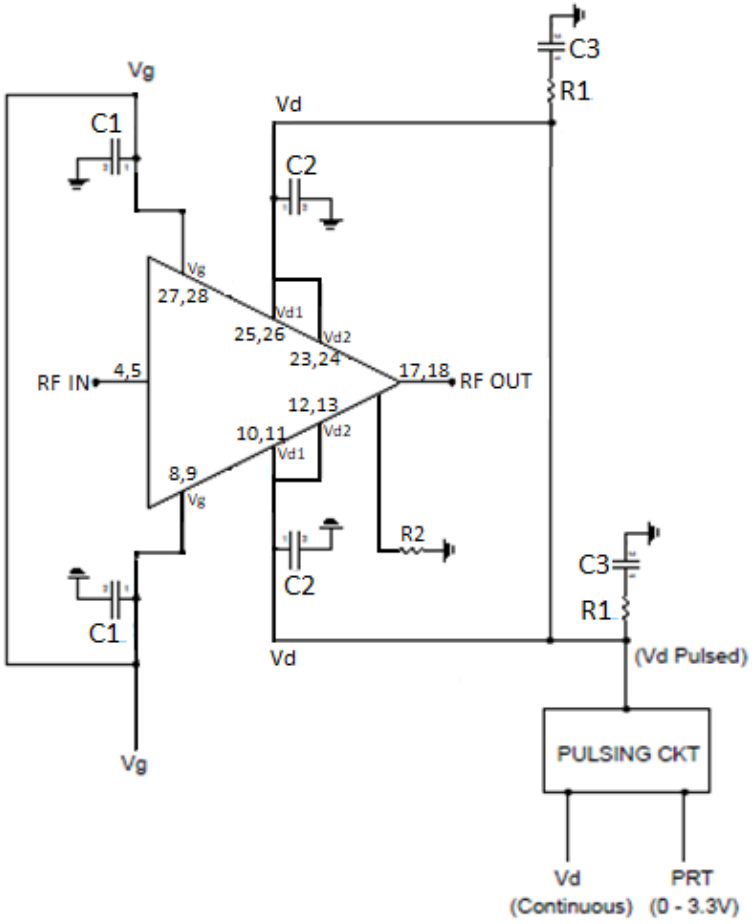
## Pin Configuration:




## Pin Description:

1. Pin no. 4,5 : RF IN (RF Input)
2. Pin no. 8,9,27,28 : Vg (Common gate voltage for 1st and 2nd Stages)
3. Pin no. 10,11,25,26 : Vd1 (1st Stage Drain Voltage)
4. Pin no. 12,13,22,23,24 : Vd2 (2nd Stage Drain Voltage)
5. Pin no. 14 : DetVout (Output Voltage of Detector)
6. Pin no. 17,18 : RF OUT (RF Output)
7. Pin no. 1,2,3,6,7,15,16 19.20,21 : GND (Ground)

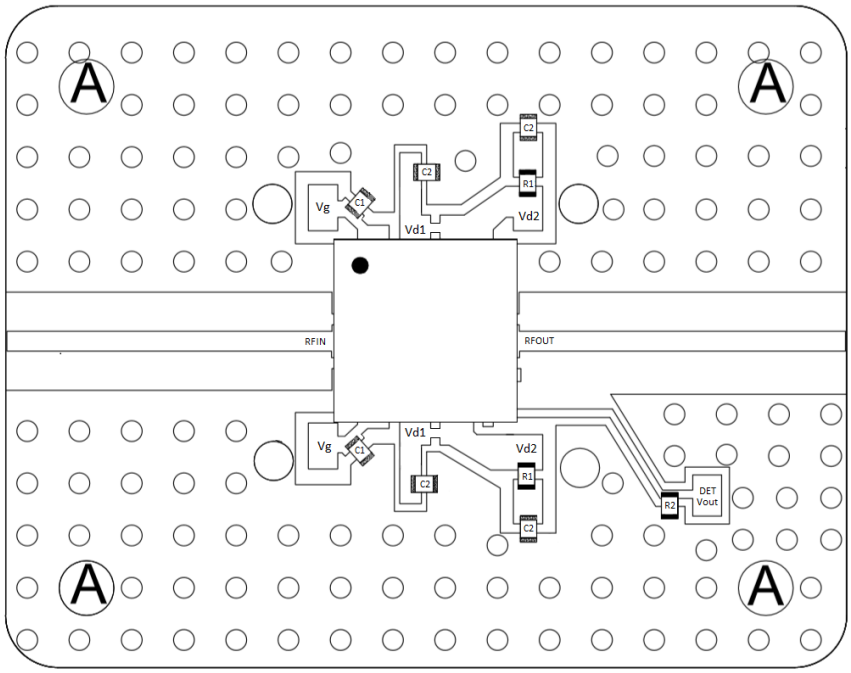
## Application Circuit for Drain Pulsing of PA:




## Off Chip Components used for the Assembly:

| Component | Part Number/Description | Vendor |
|---|---|---|
| 1kpF MLC (C1) | VJ0402Y102KNAAJ/1kpF±10%;25V or Equivalent | Vishay |
| 10kpF MLC (C2,C3) | VJ0402Y103KNAAJ/10kpF±10%;25V or Equivalent | Vishay |
| 2.2ohm (R1) | CRCW04022R20JNTD/2.2ohm±1%;0.063W or Equivalent | Vishay |
| 10kohm (R2) | CRCW040210K0FKEDC/10kohm±1%;0.063W or Equivalent | Vishay |

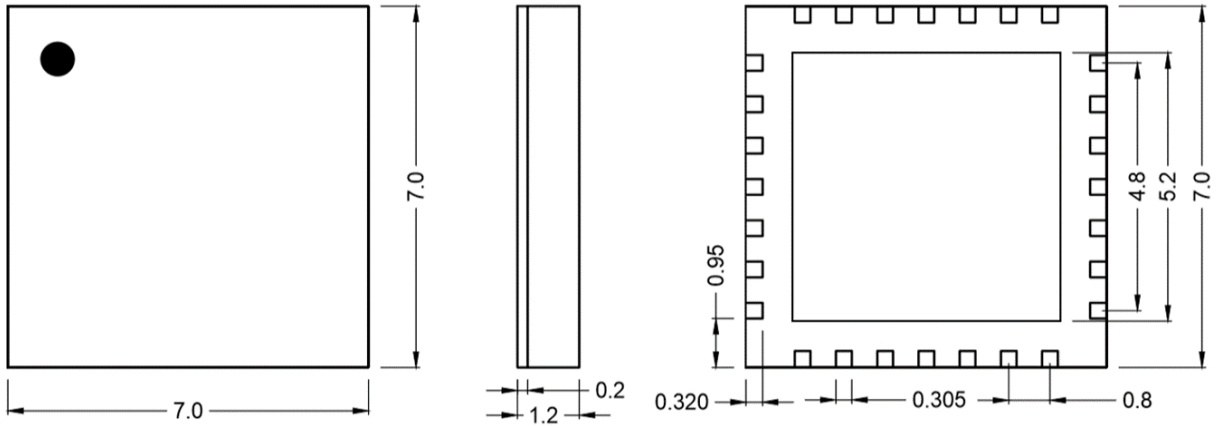
## Recommended PCB Drawing:




**Note:**

1. Input and output 50 ohm lines are preferably on 10 mil RT Duroid substrate.
2. Gate Bypass Capacitor “C1” and the Drain Bypass Capacitor “C2” need to be placed close to the chip.
3. Input and Output ports are DC decoupled ports.
4. Use high thermal conductive material for mounting of the chip for long term reliability.

## Package Mechanical Details:




## Package Description:

1. Body: Plastic - Semiconductor Grade.
2. Lead Frame: Copper, 194 FH.
3. Lead Finish: Full Gold Plate (Gold on Nickel Plating).
4. Frame Thickness: 0.2030 ± 0.0076.
5. JEDEC Outline: MO-220 (VKKV).
6. All Dimension mentioned are in mm (millimeters).

***GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing***

All information and Specifications are subject to change without prior notice. Before using the product, please download and refer to datasheet from website.